

FIG. 1

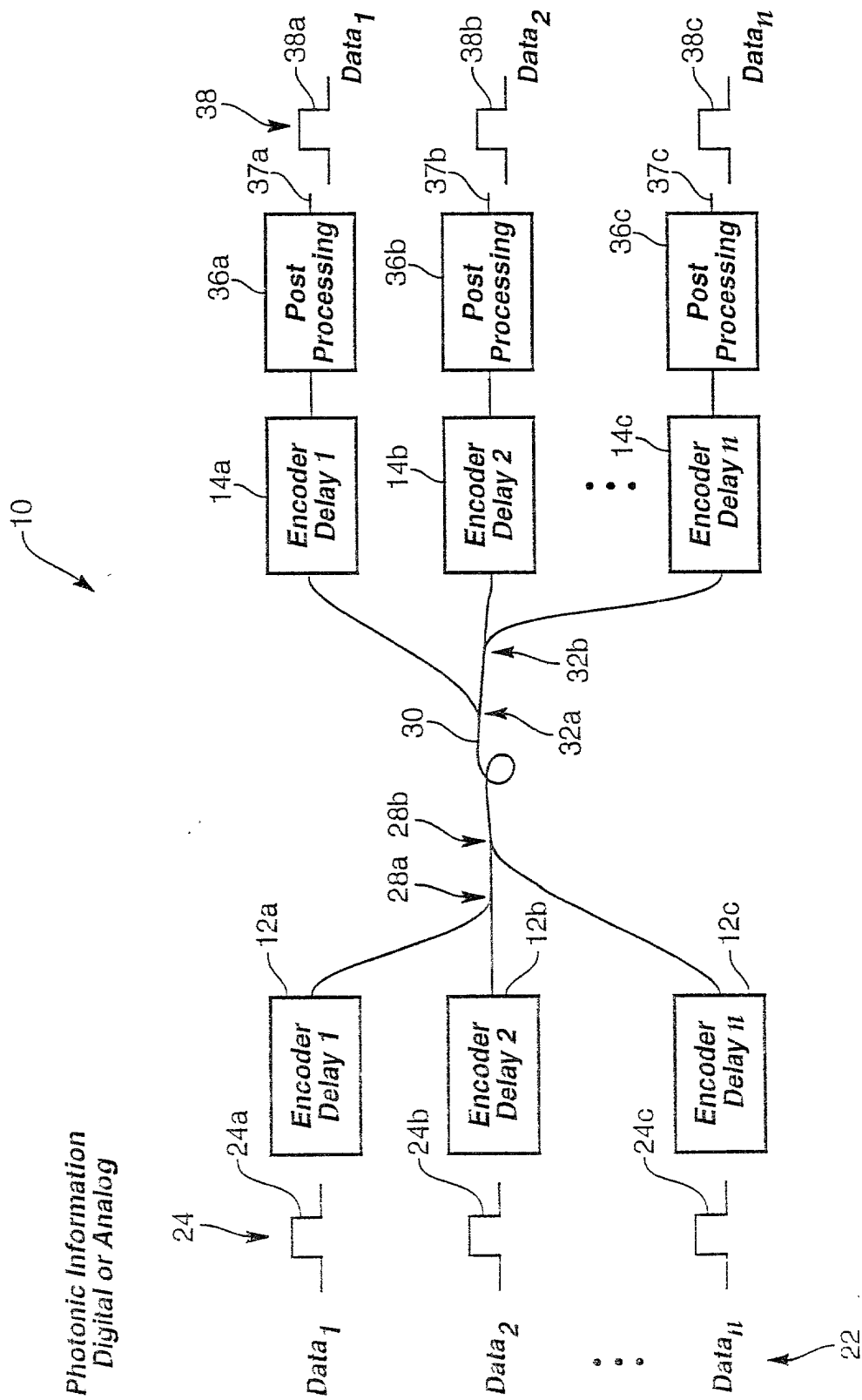
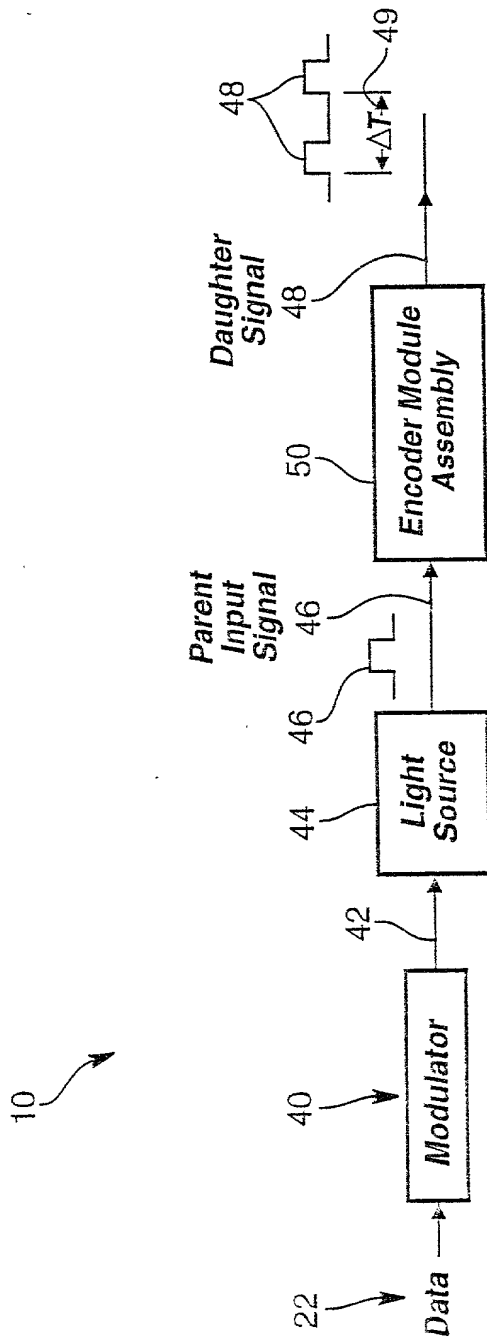


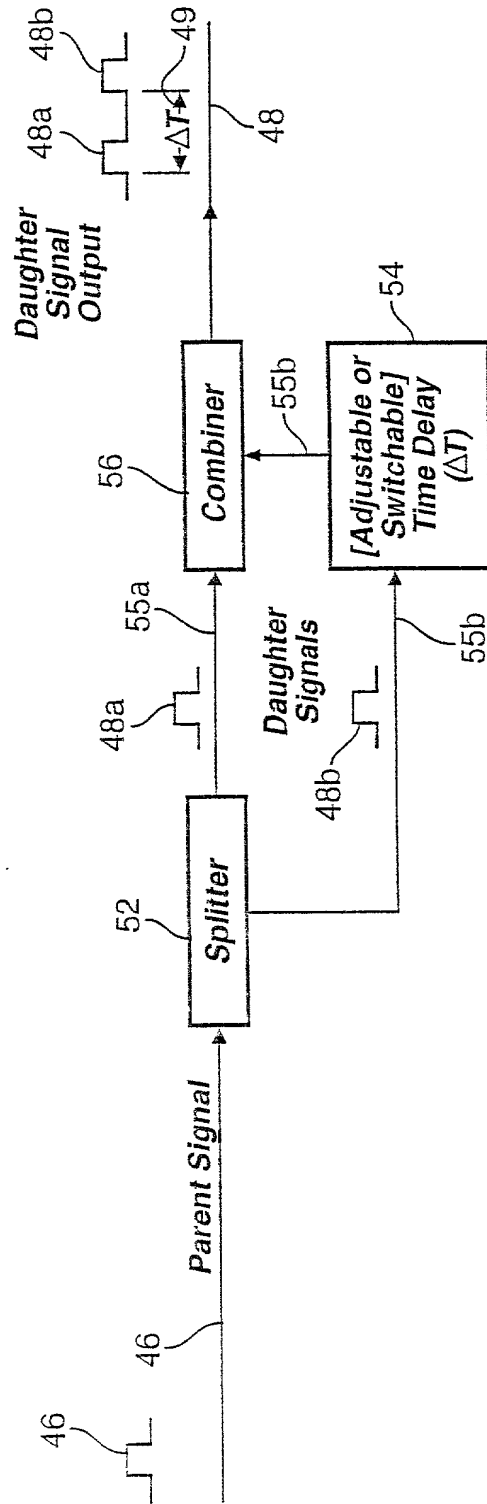
Fig. 2



Differential Delay Multiplexer Sender/Encoder

Fig. 3

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Differential Delay Multiplexer (DDM) Sender/Encoder

Fig. 4

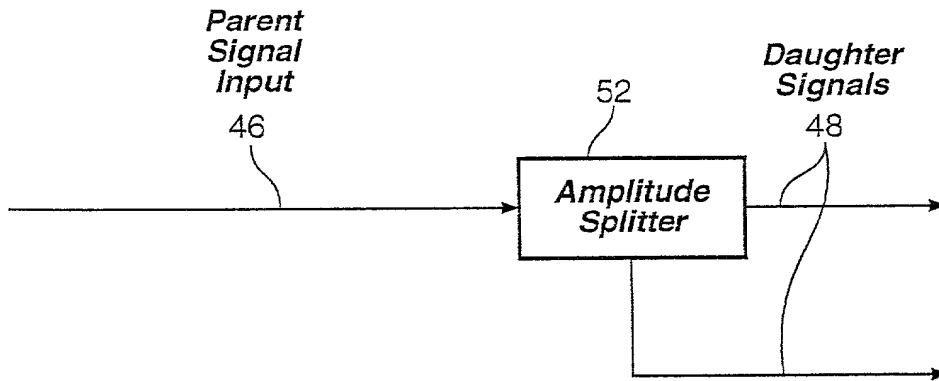
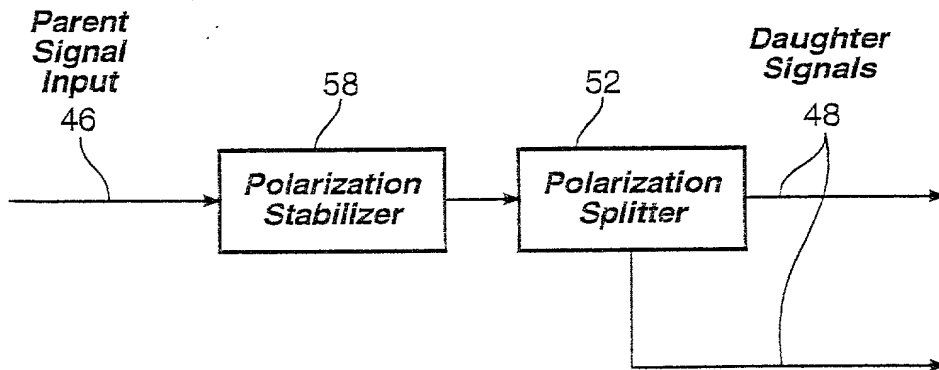
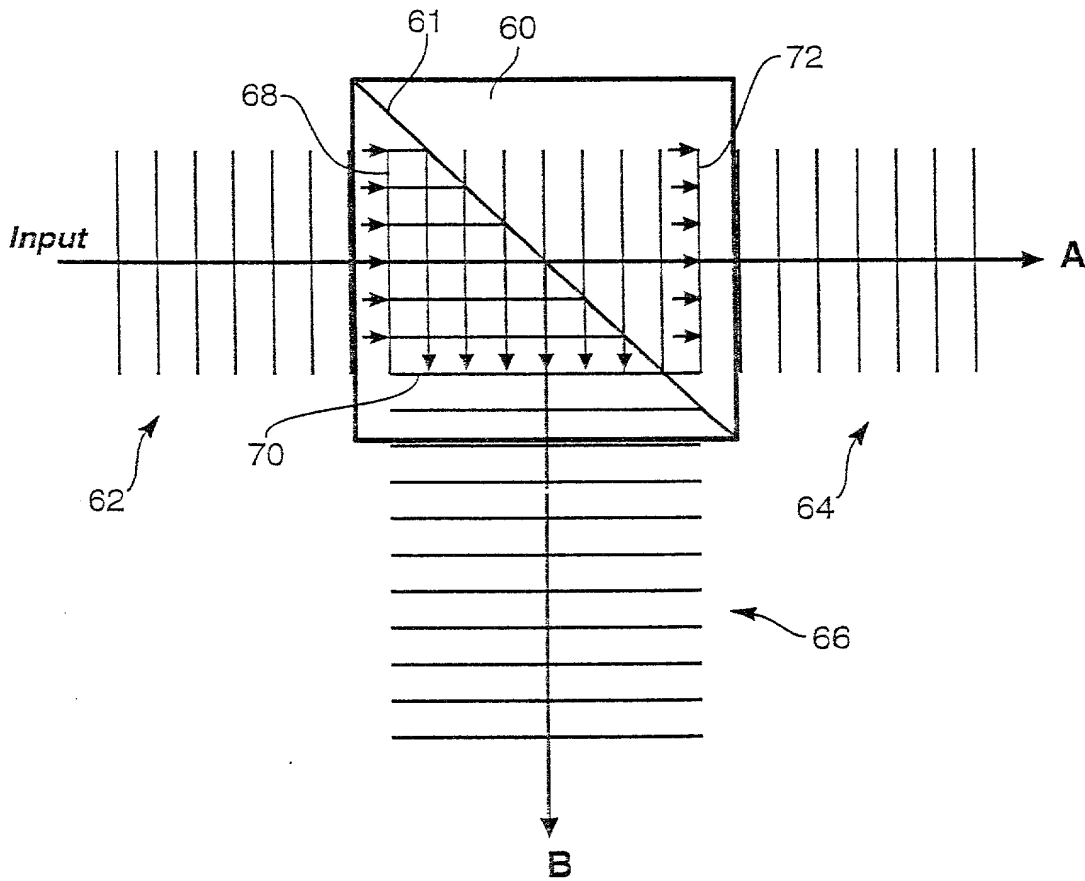


FIG. 5



Splitting Criteria

FIG. 6



Amplitude or Polarization Splitter

FIG. 7

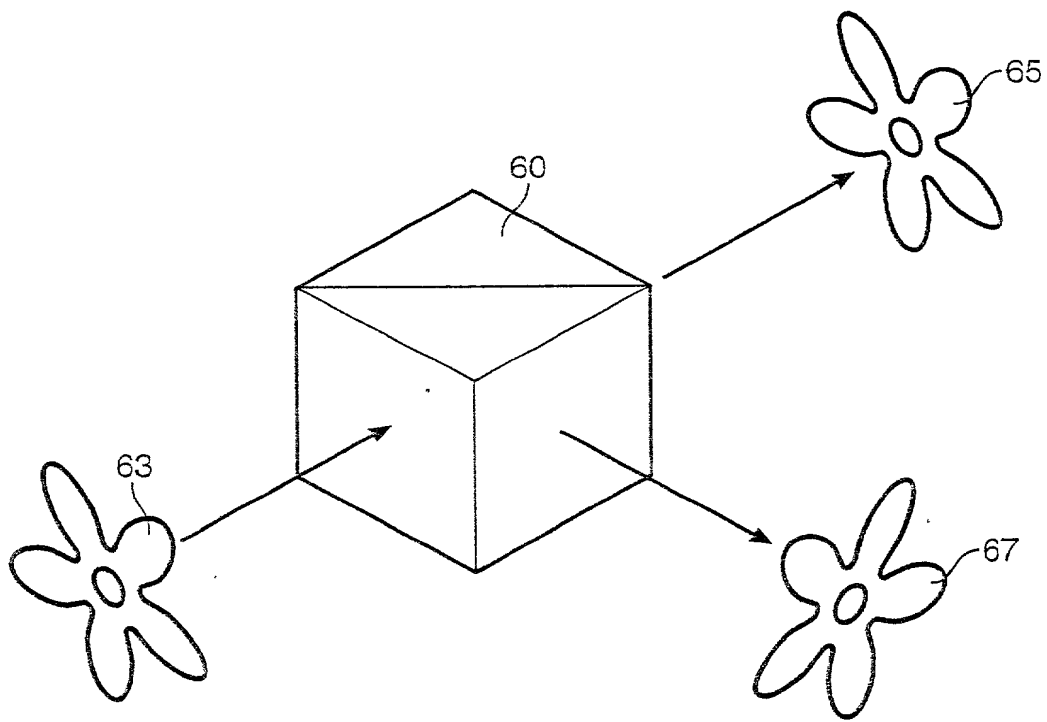
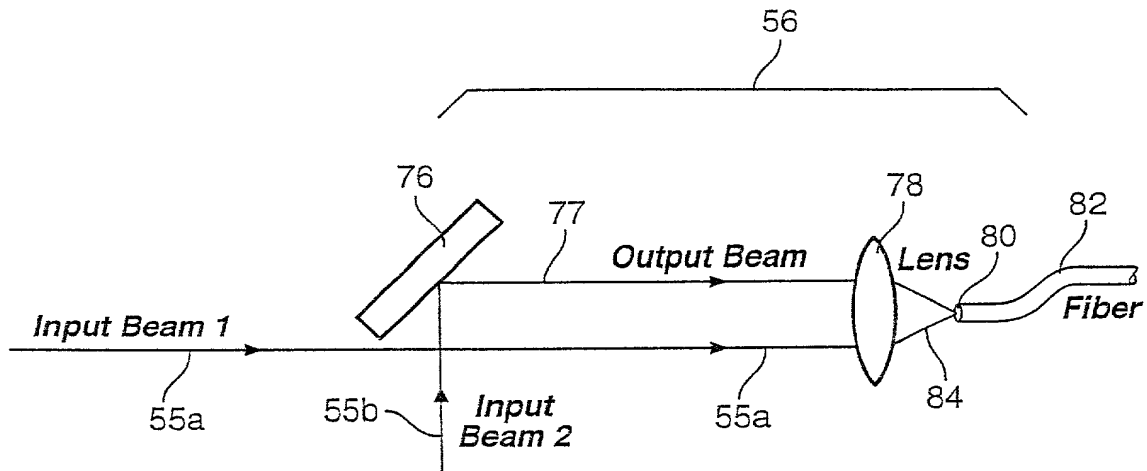


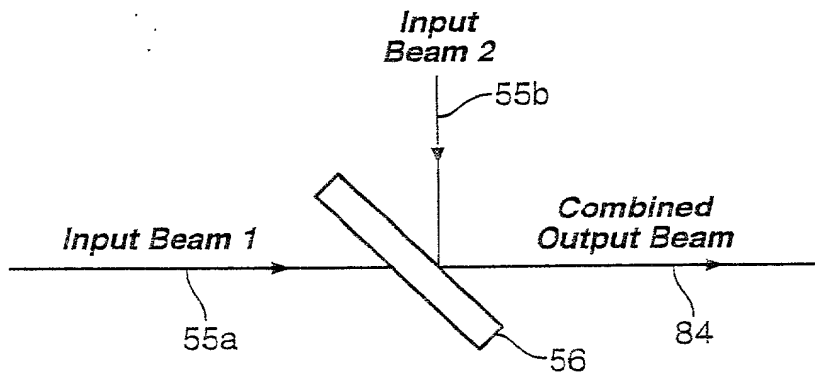
Image Signals Which
Maintain Spatial Information

FIG. 7A

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Beam Combiner
FIG. 8



Amplitude or Polarization Combiner

FIG. 9

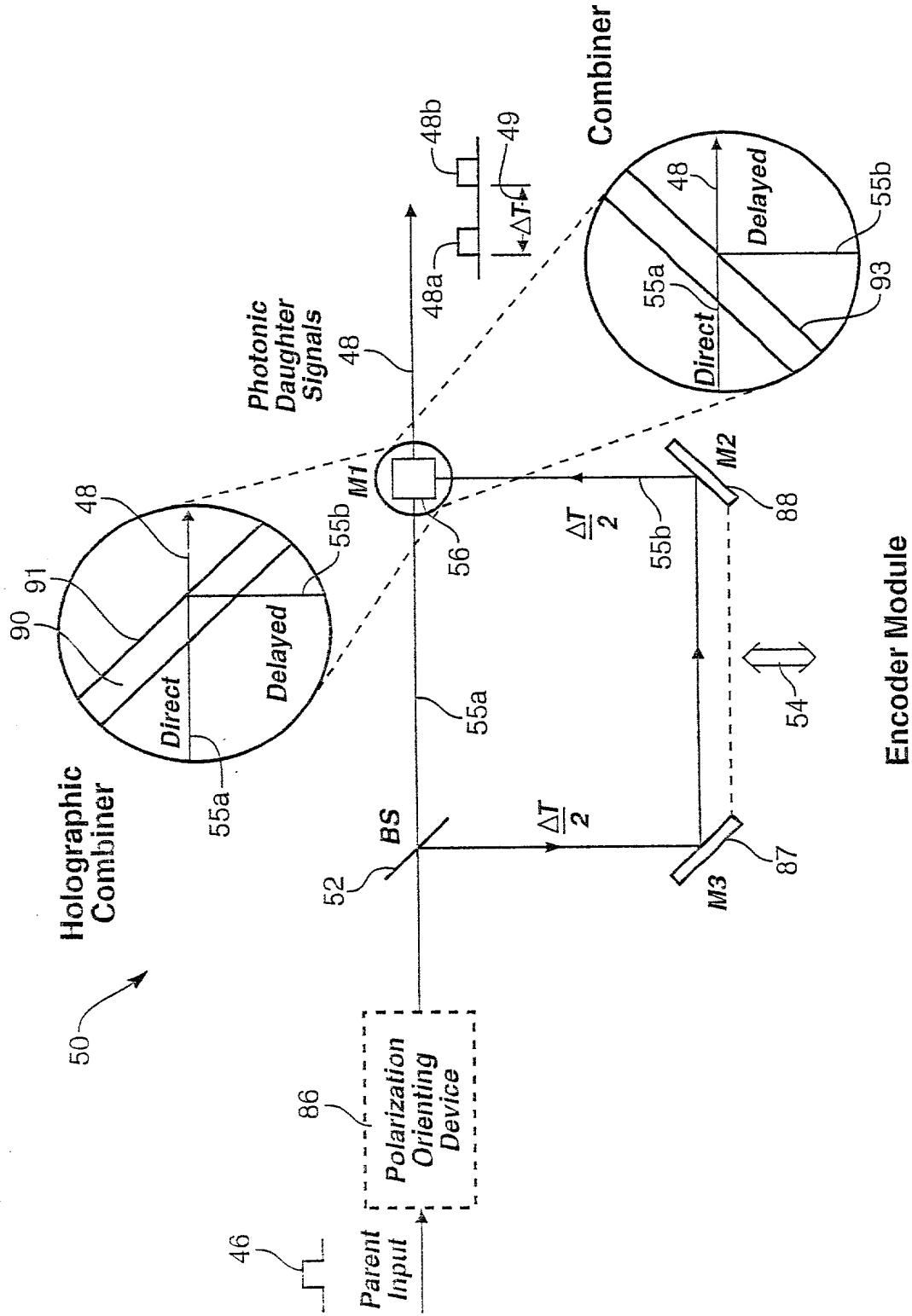


Fig. 10

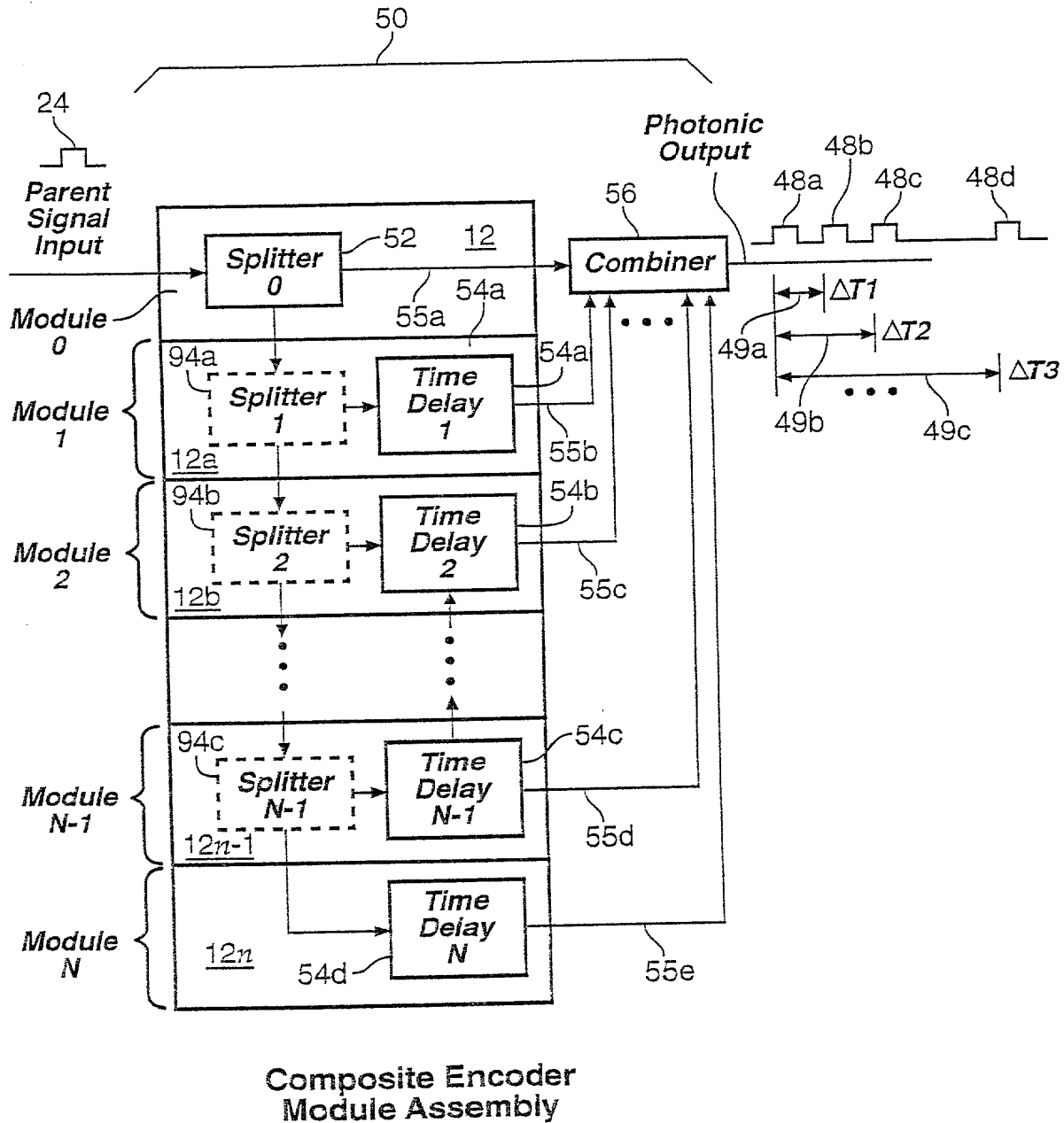


FIG. 11

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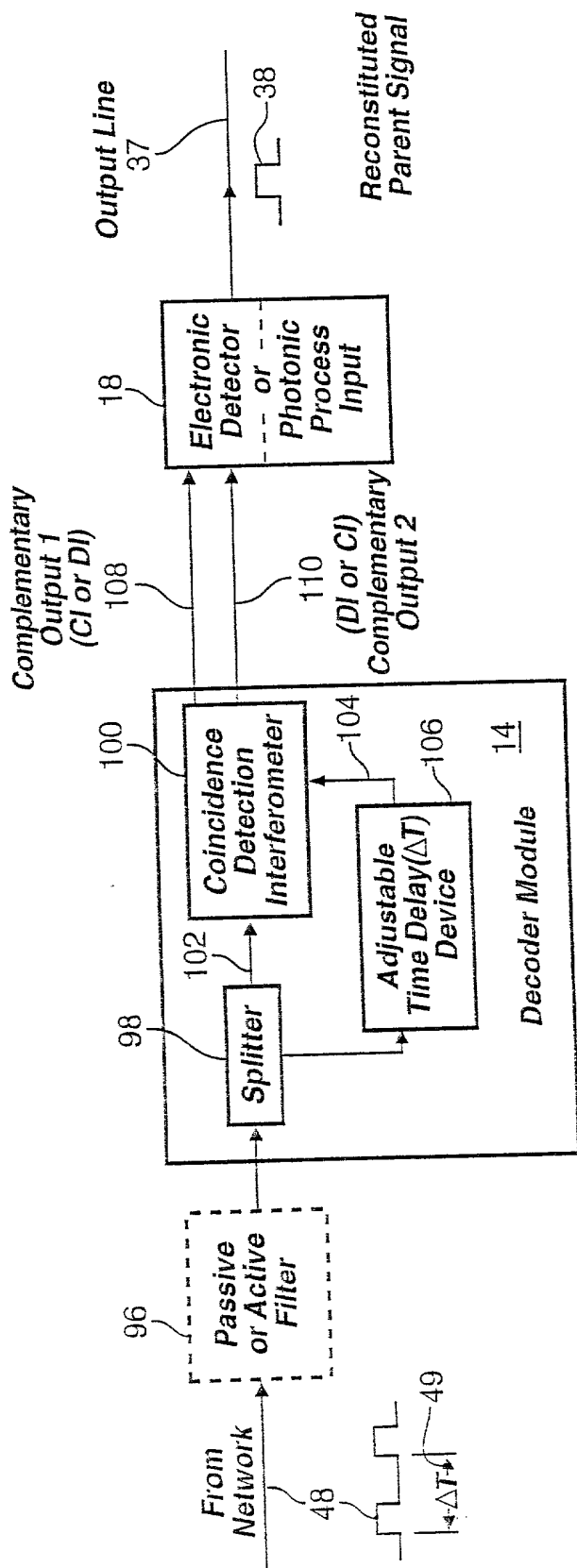


Fig. 12

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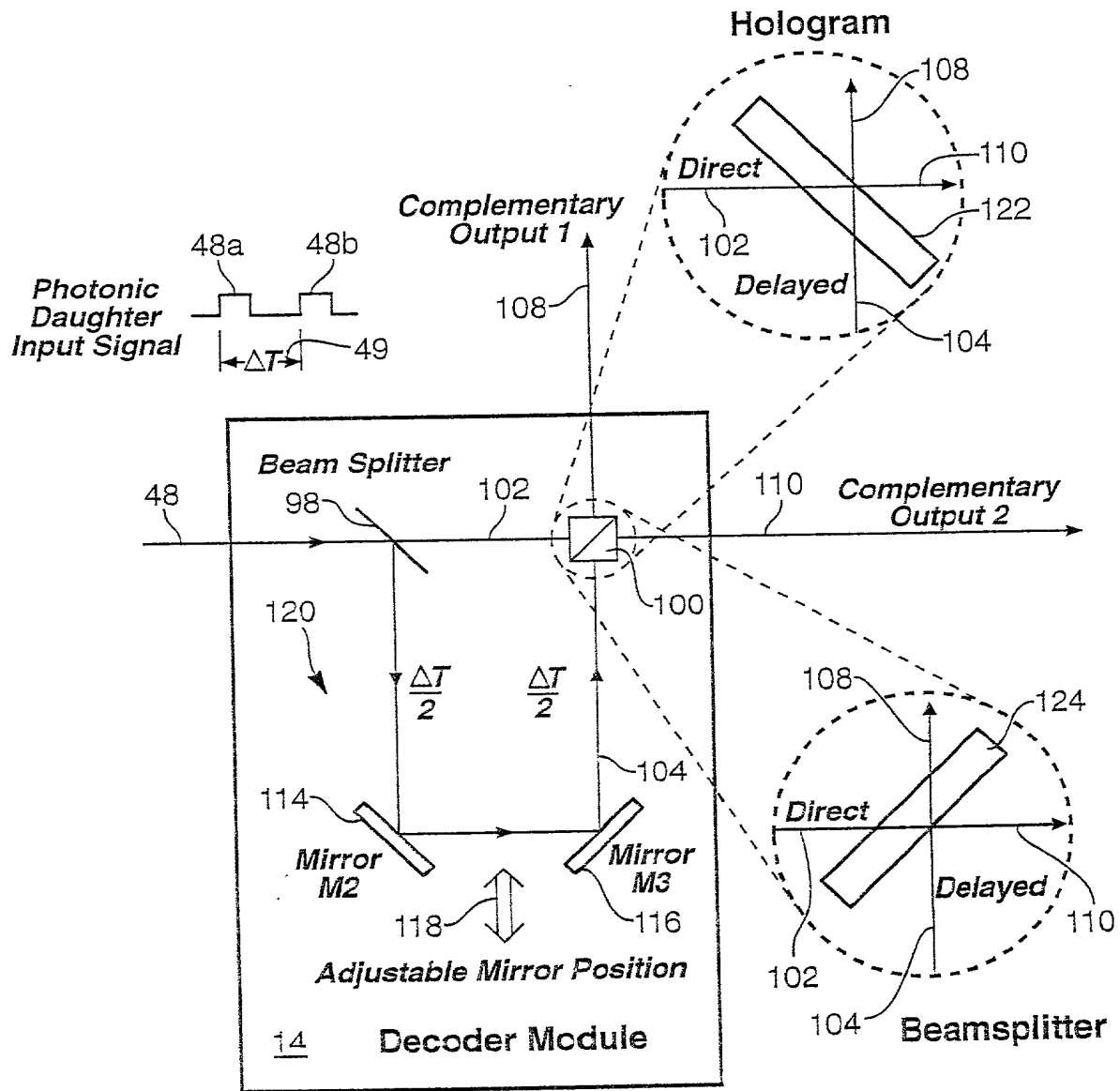


FIG. 13

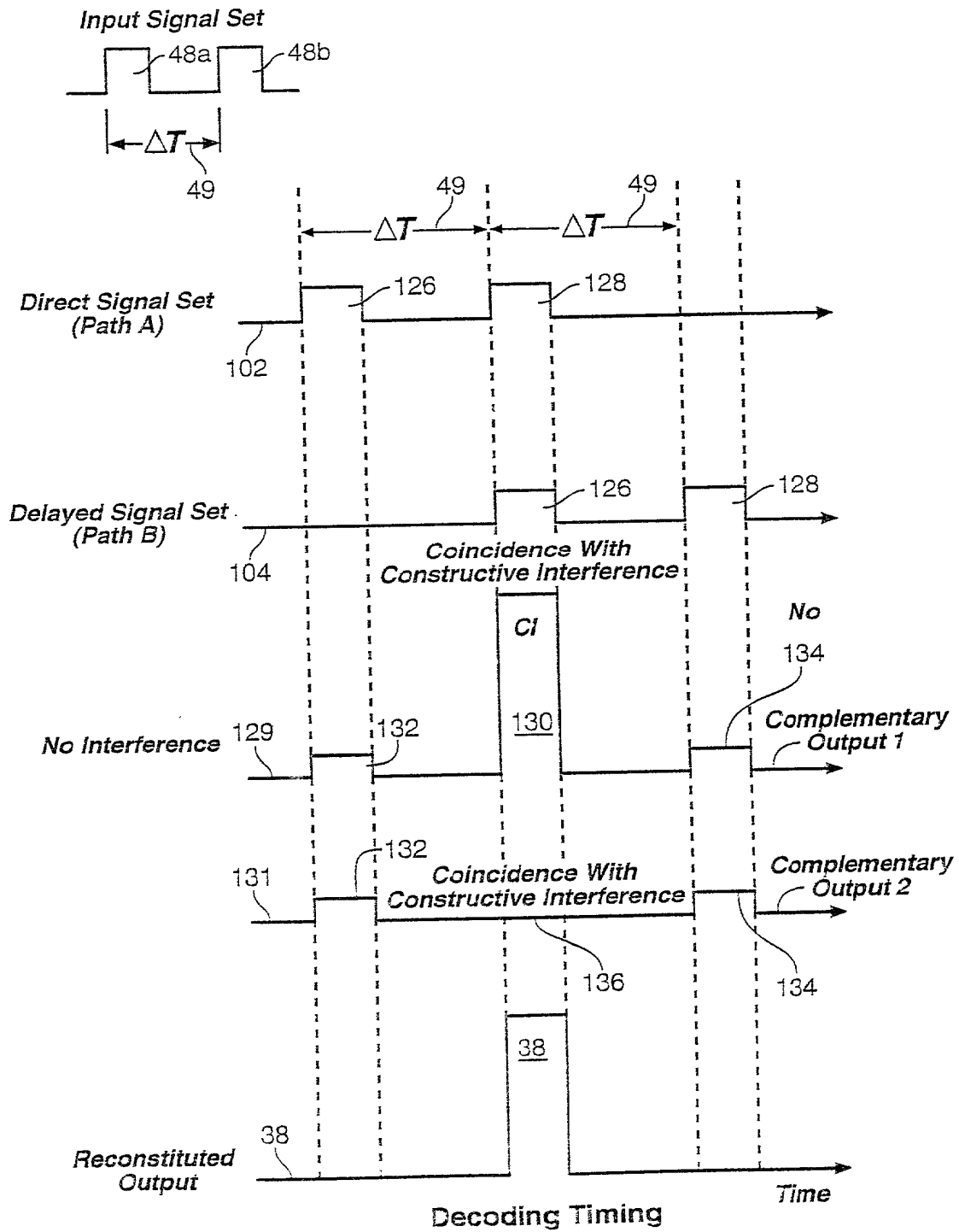


FIG. 14

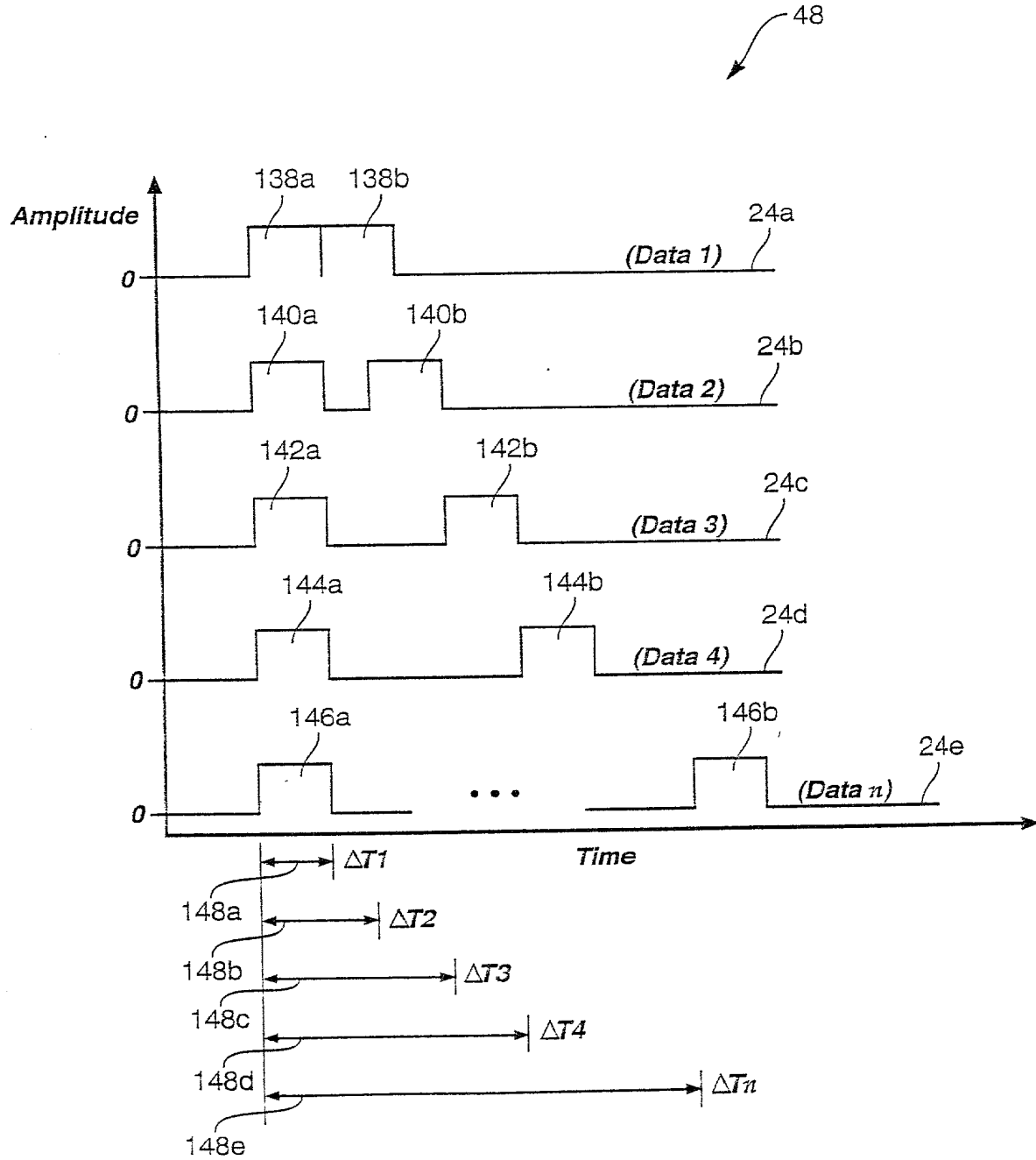


Fig. 15

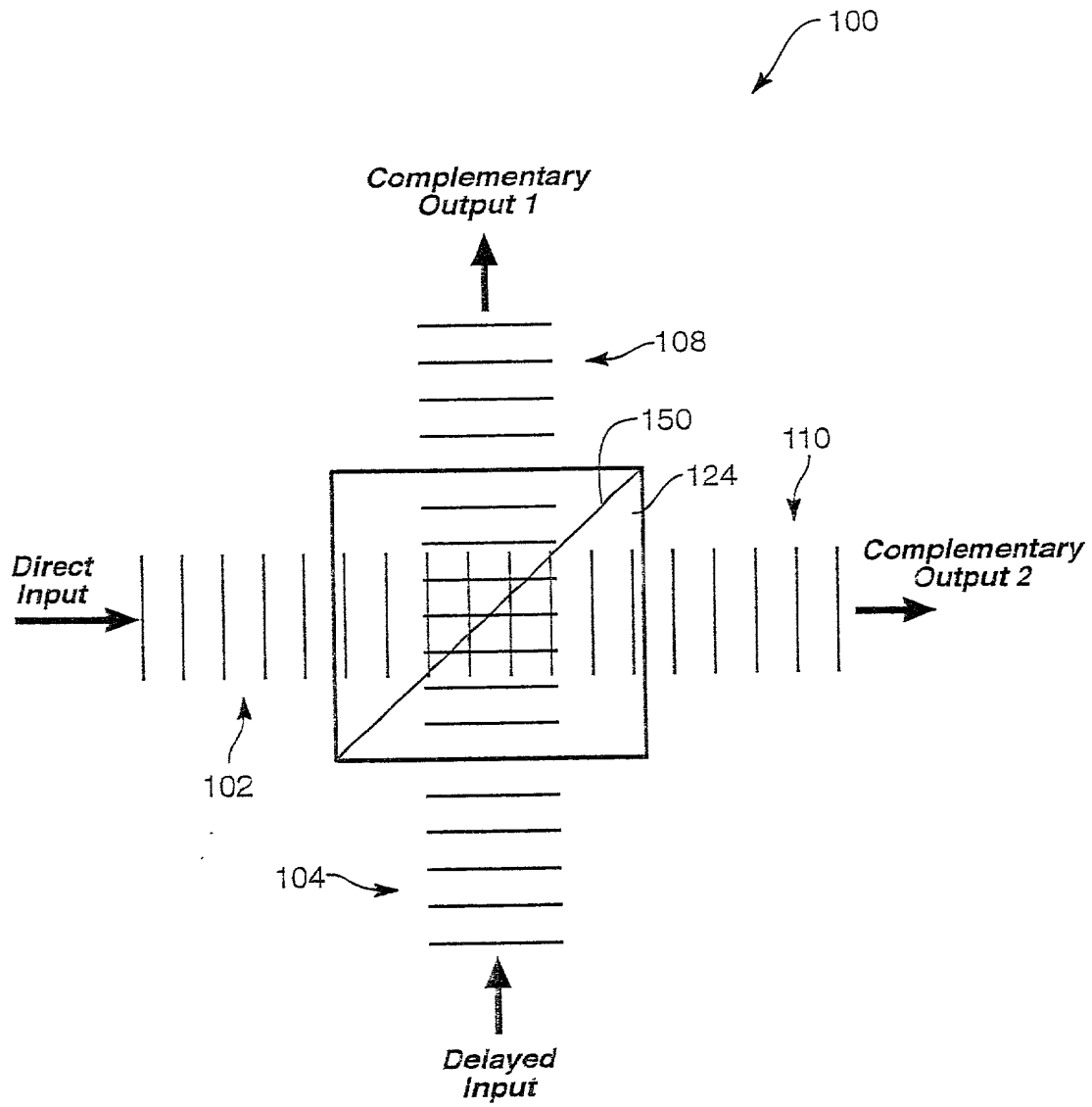


Fig. 16

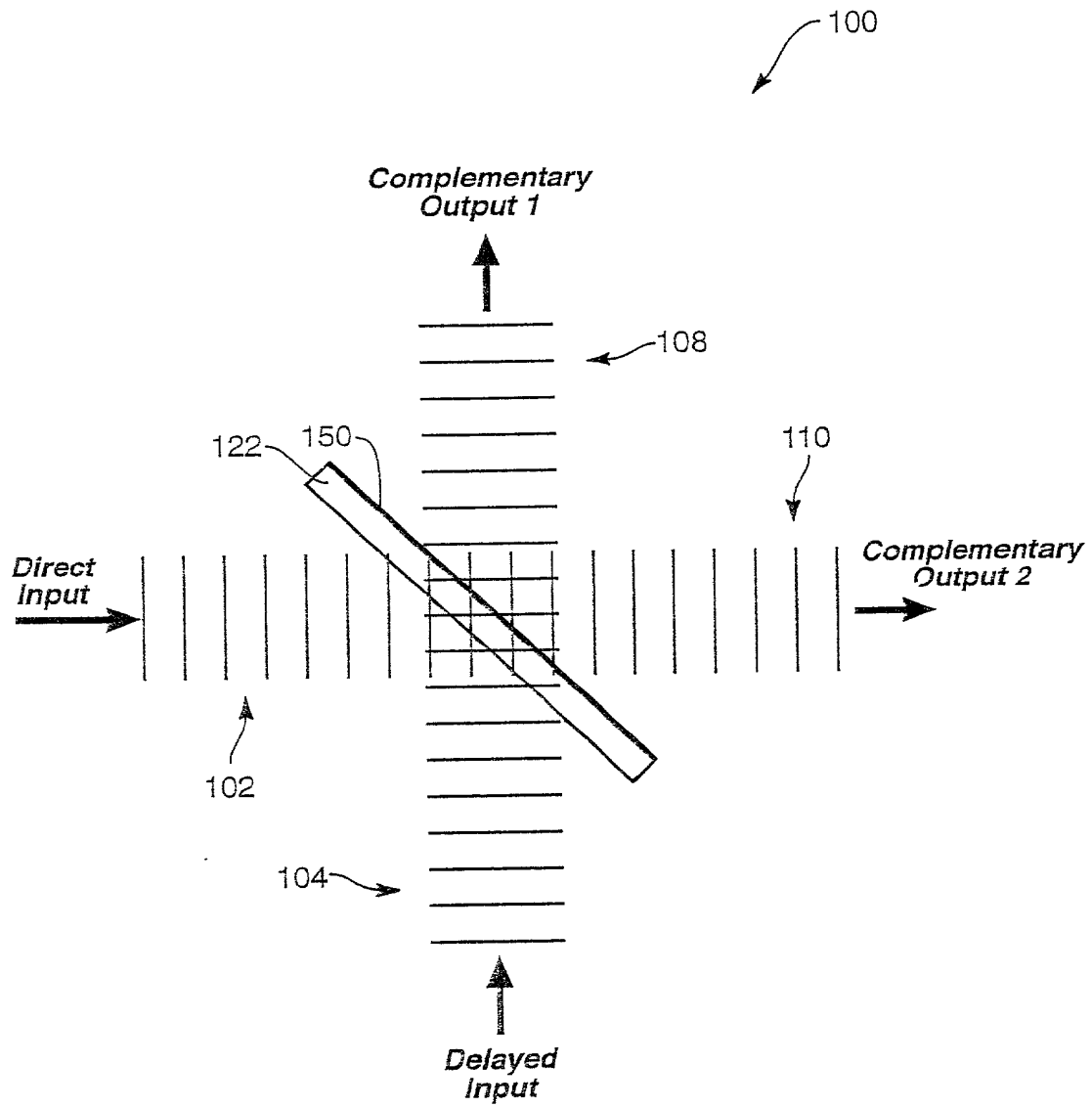


Fig. 17

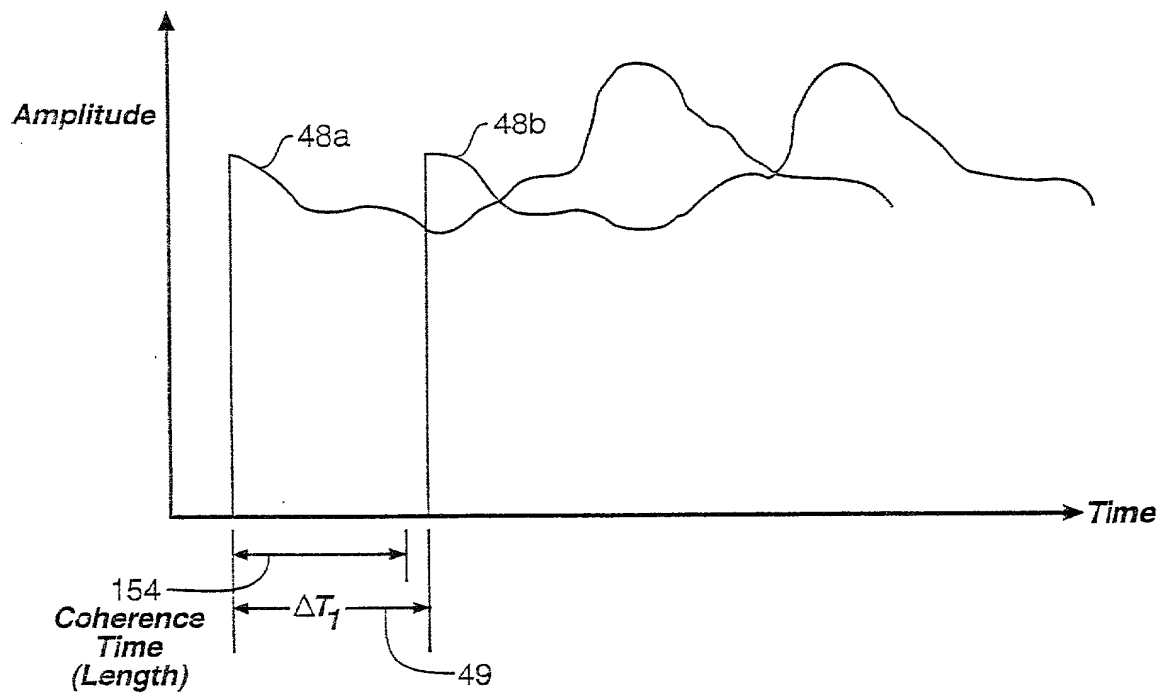


Fig. 18

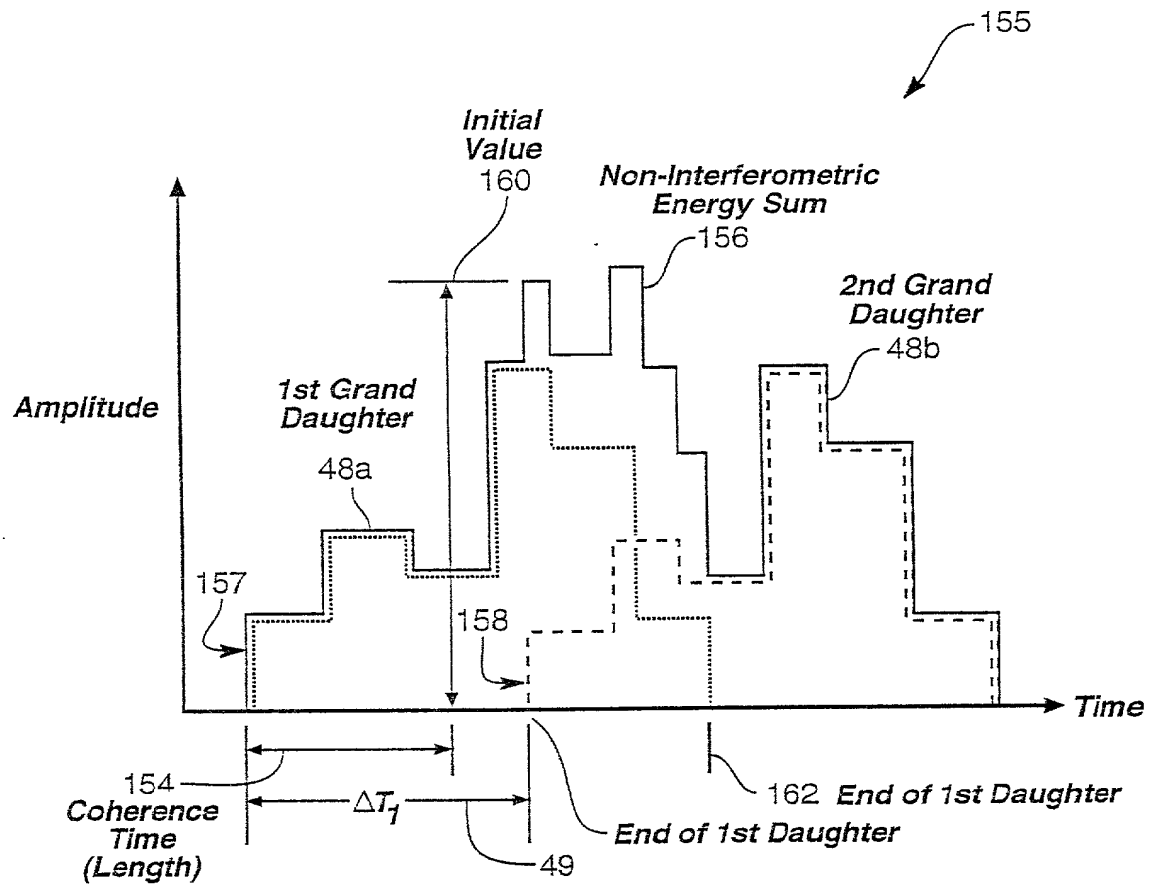


Fig. 19

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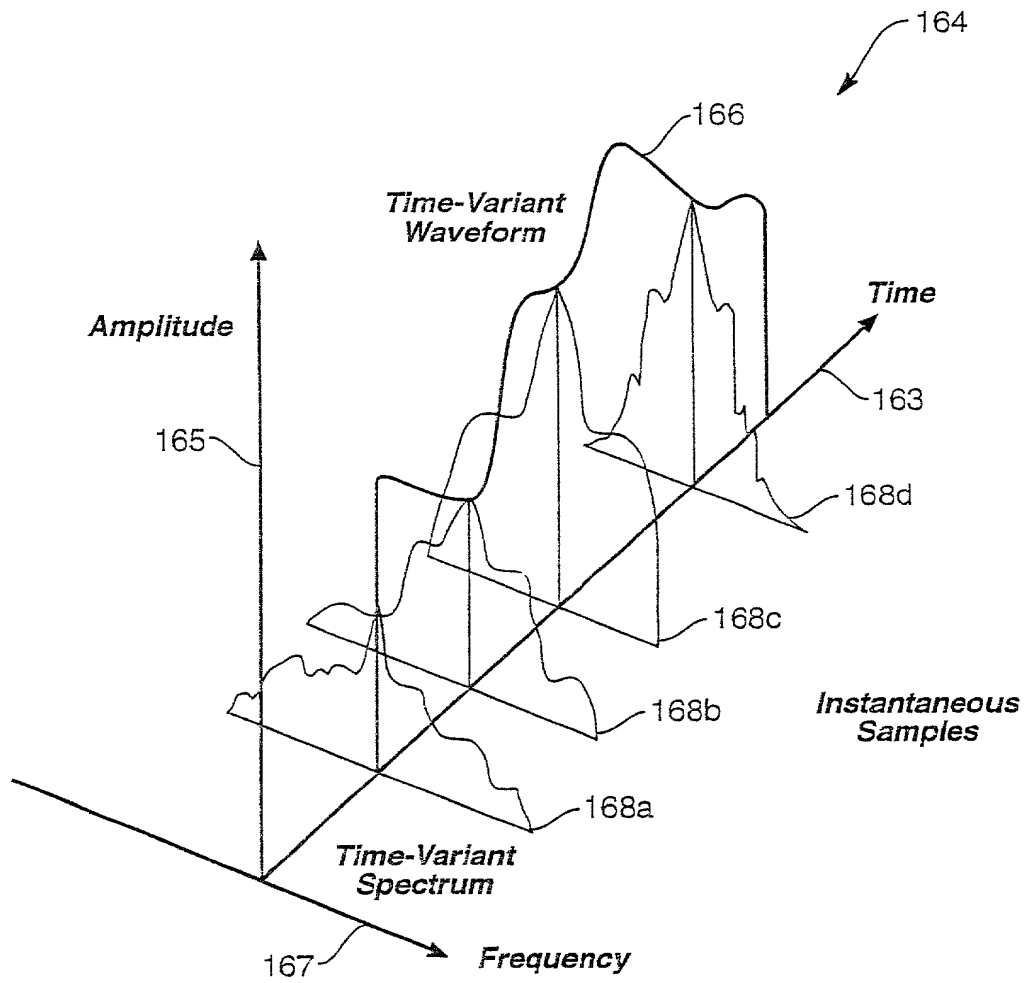


Fig. 20

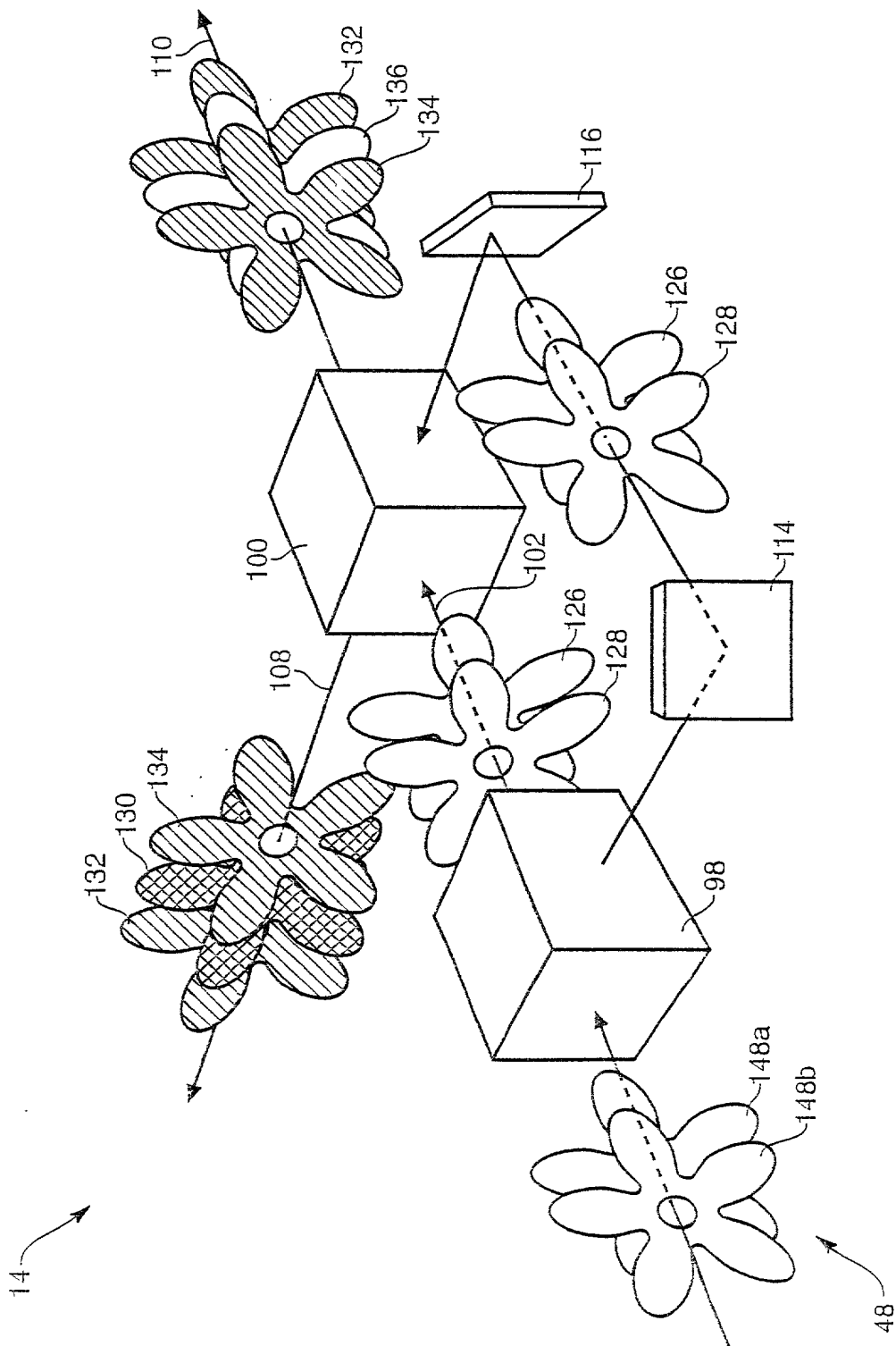
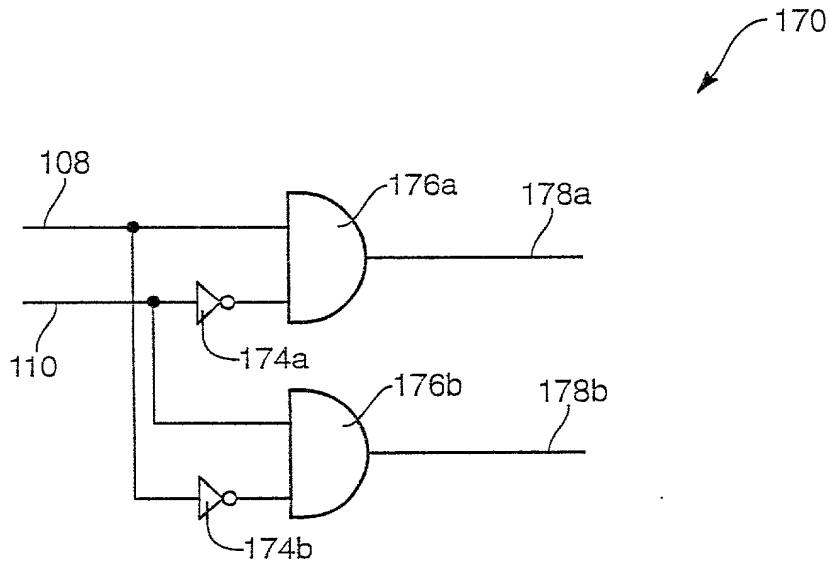
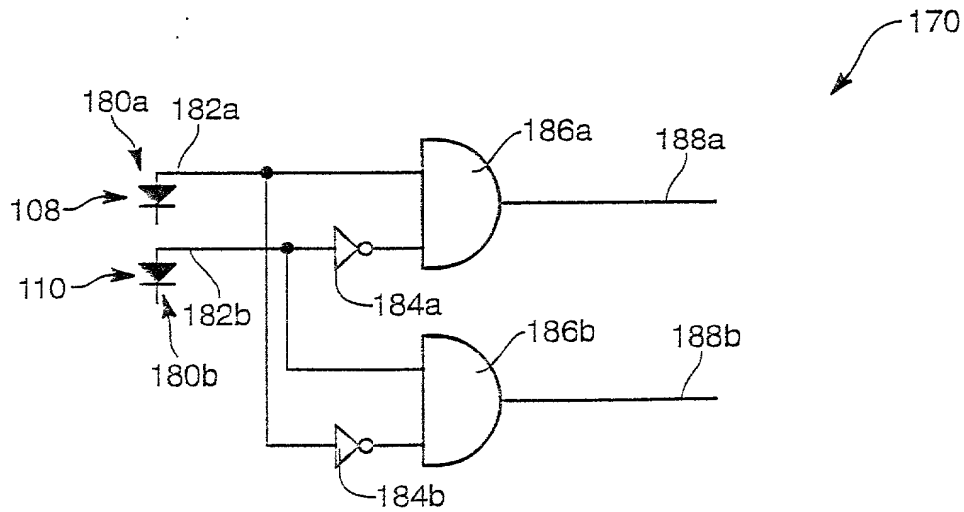


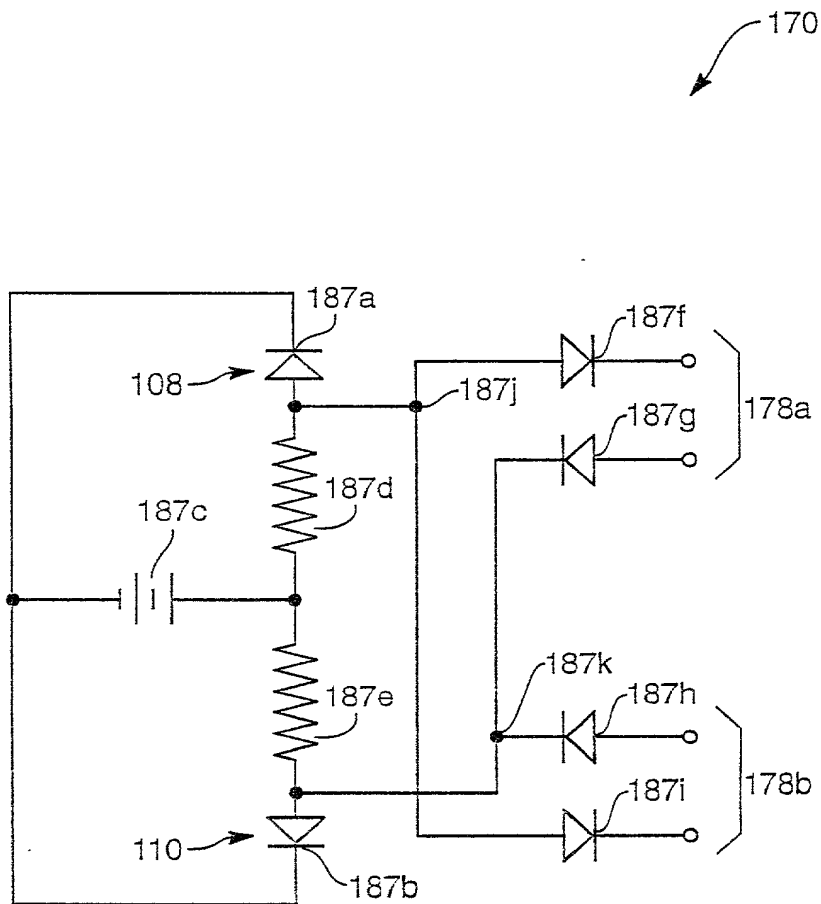
Fig. 21



Photonic Processor
Fig. 22

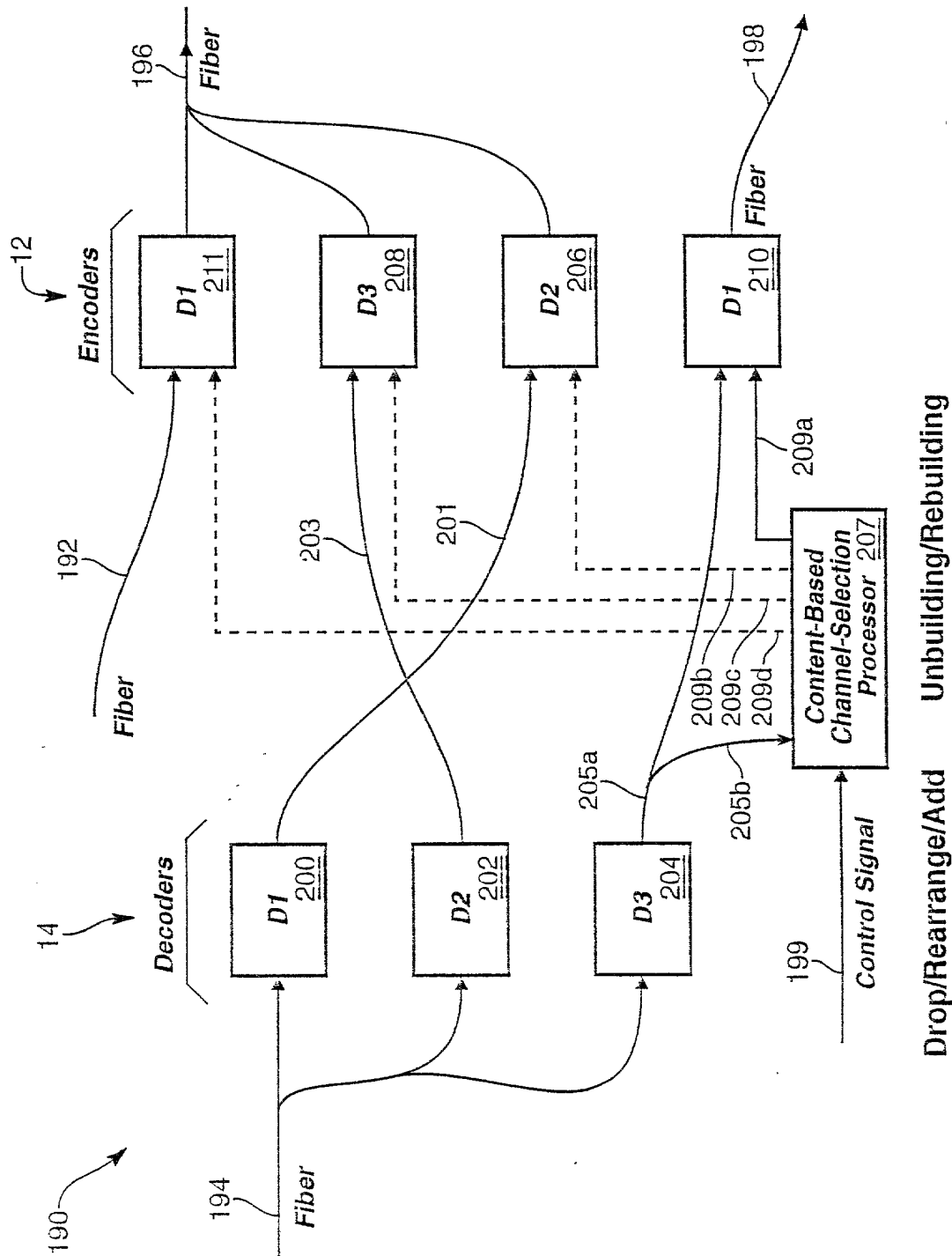


Electronic Processor
Fig. 23A



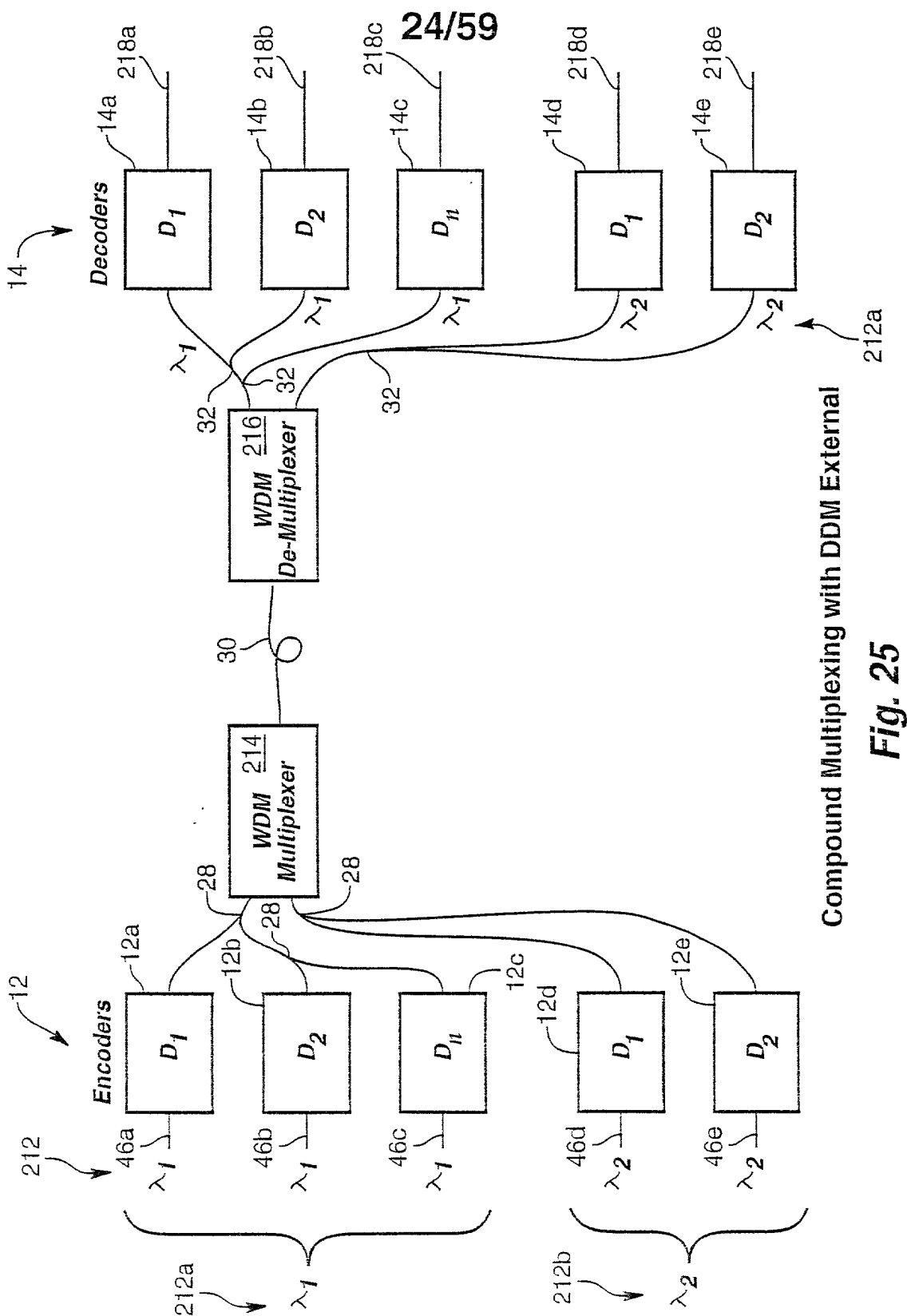
Electronic Processor

Fig. 23B



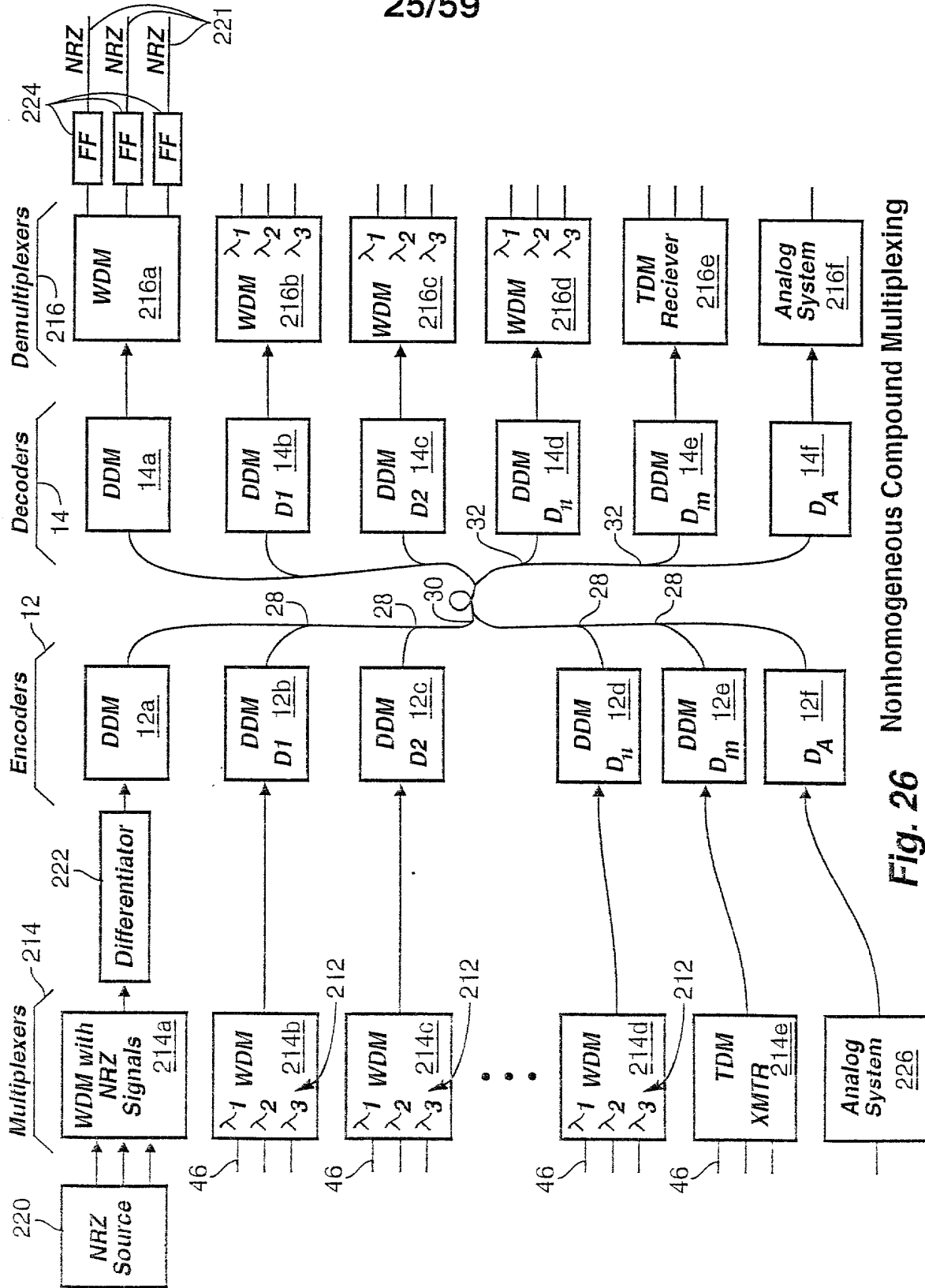
Drop/Rearrange/Add Unbuilding/Rebuilding

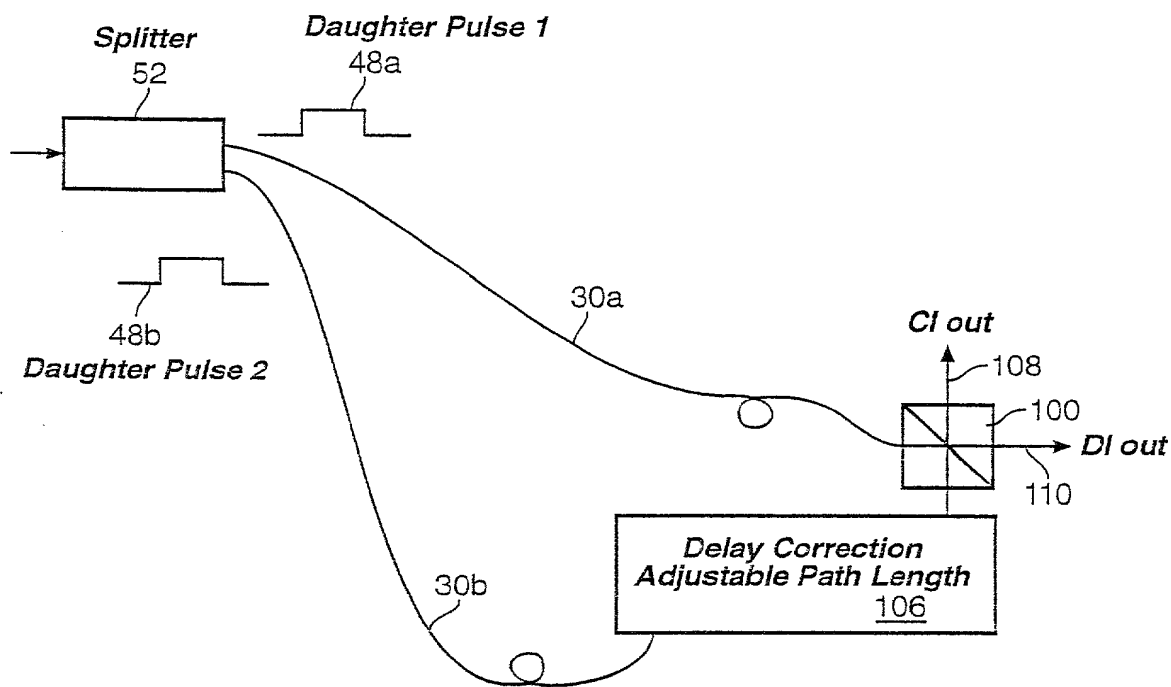
Fig. 24



Compound Multiplexing with DDM External

Fig. 25





Multiple Delay Path

Integrated Delay and
Delay Correction

FIG. 27

Photonic NRZ Interface

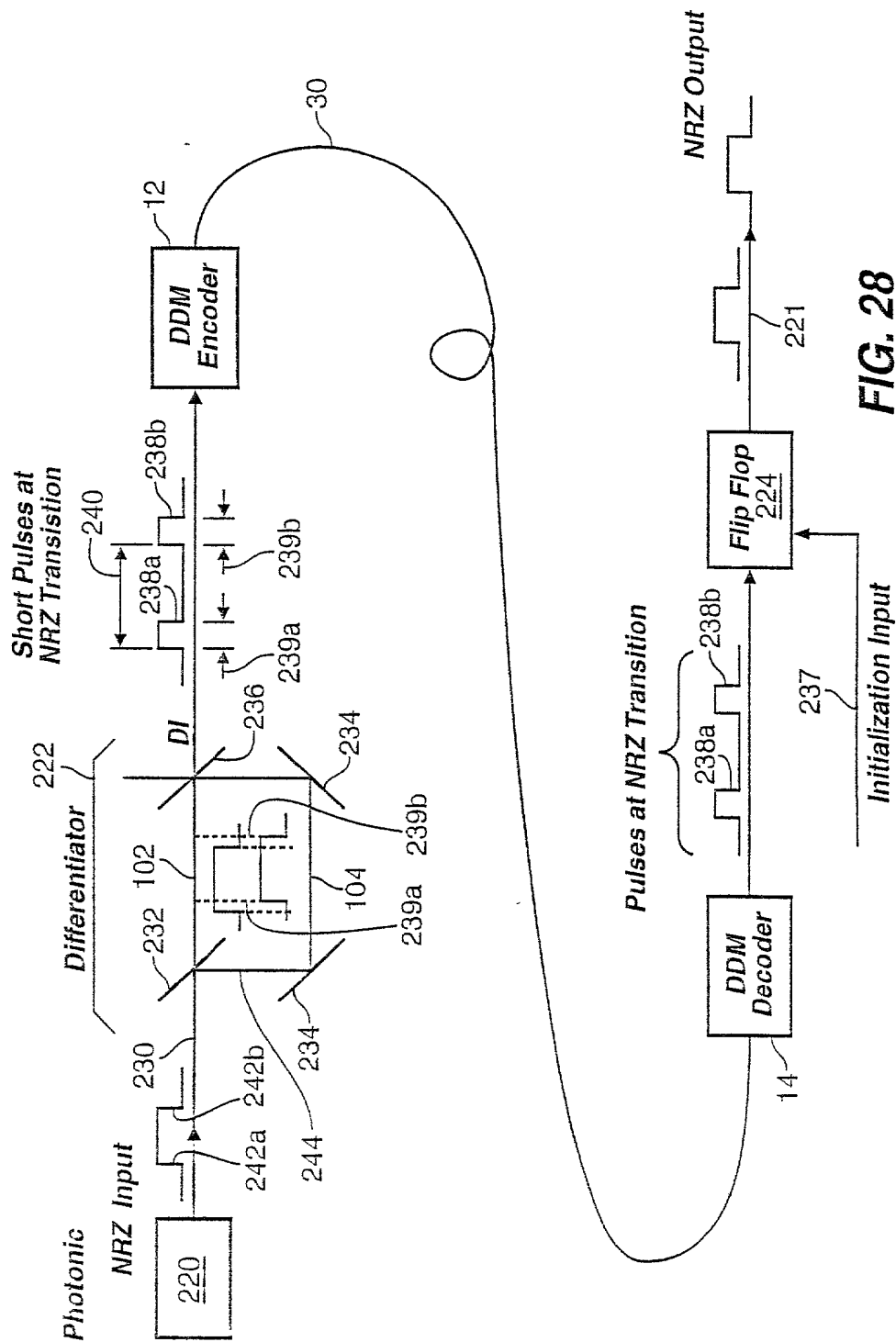


FIG. 28

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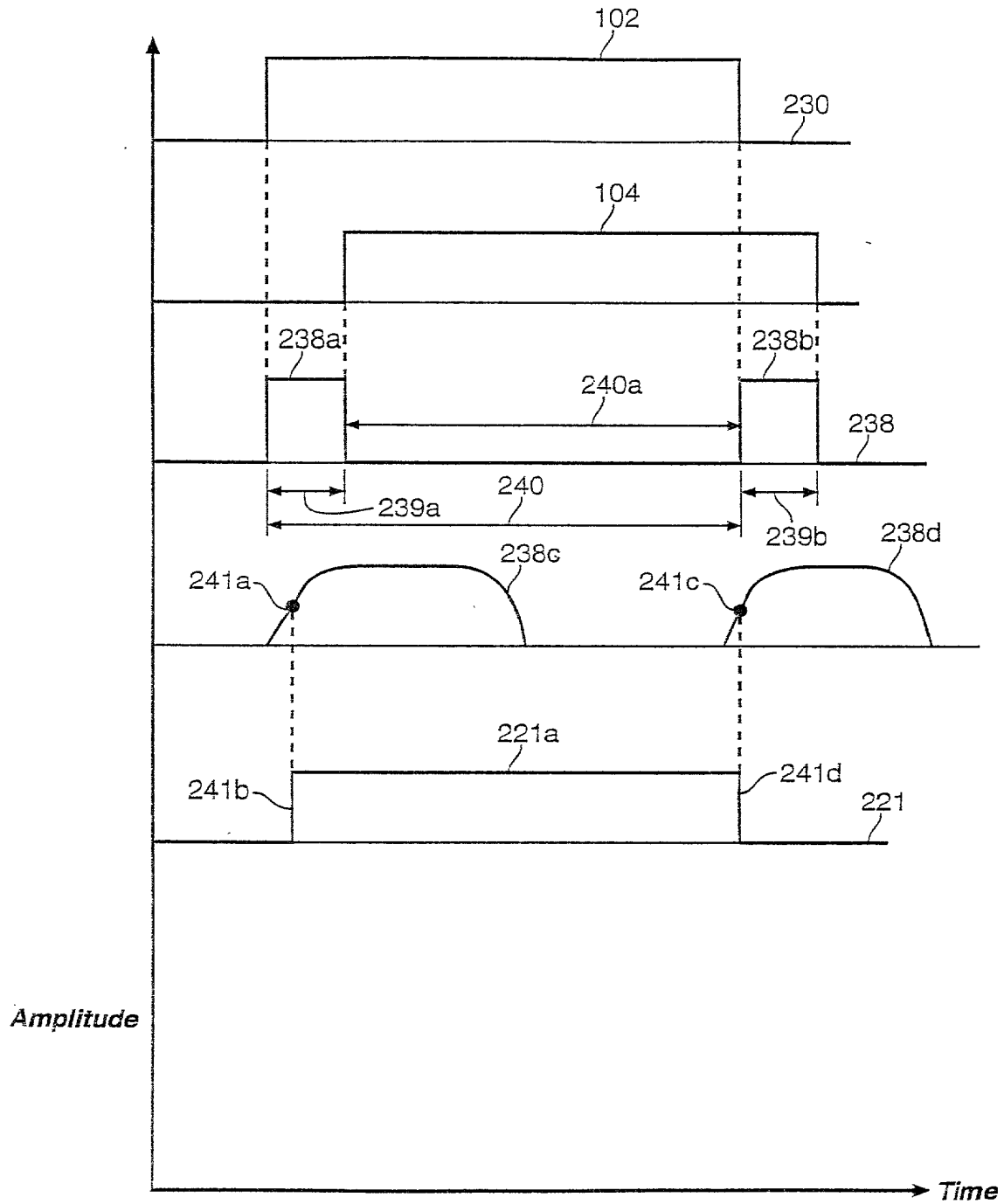
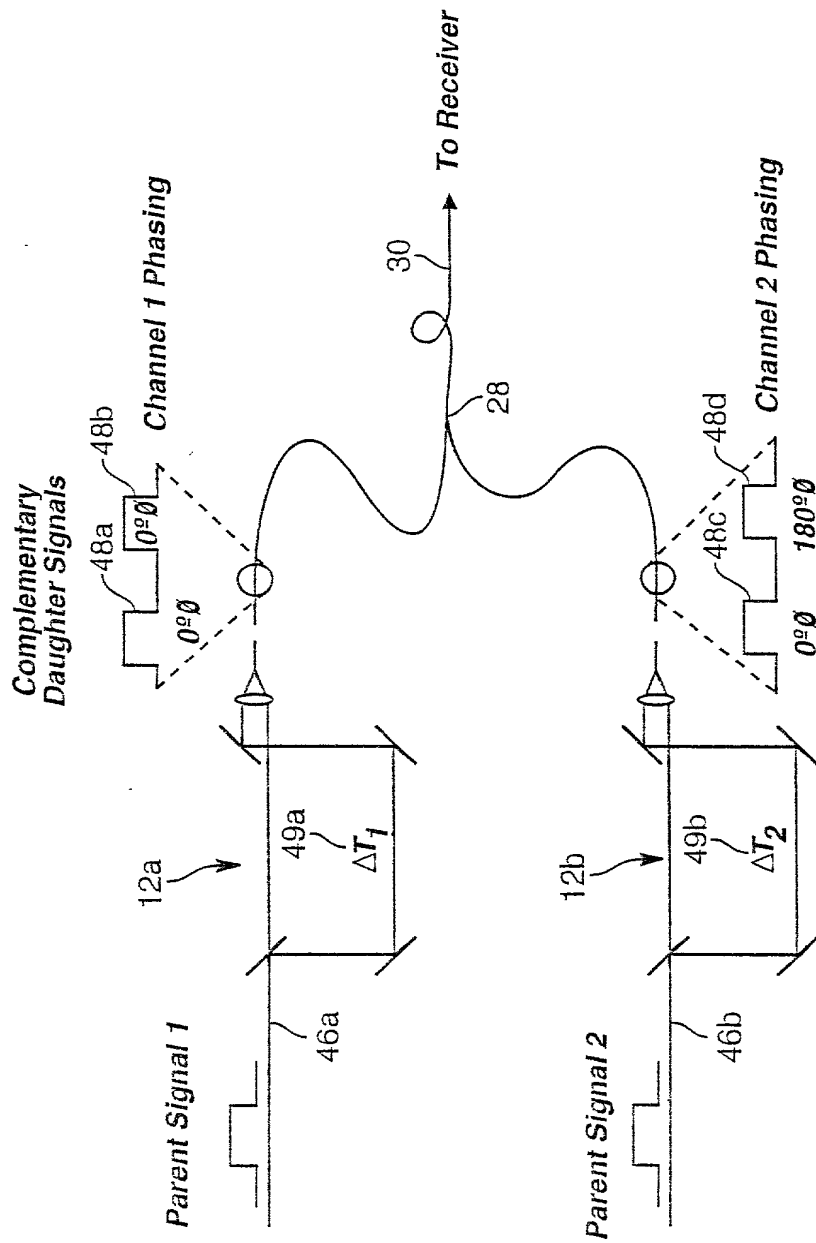


FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

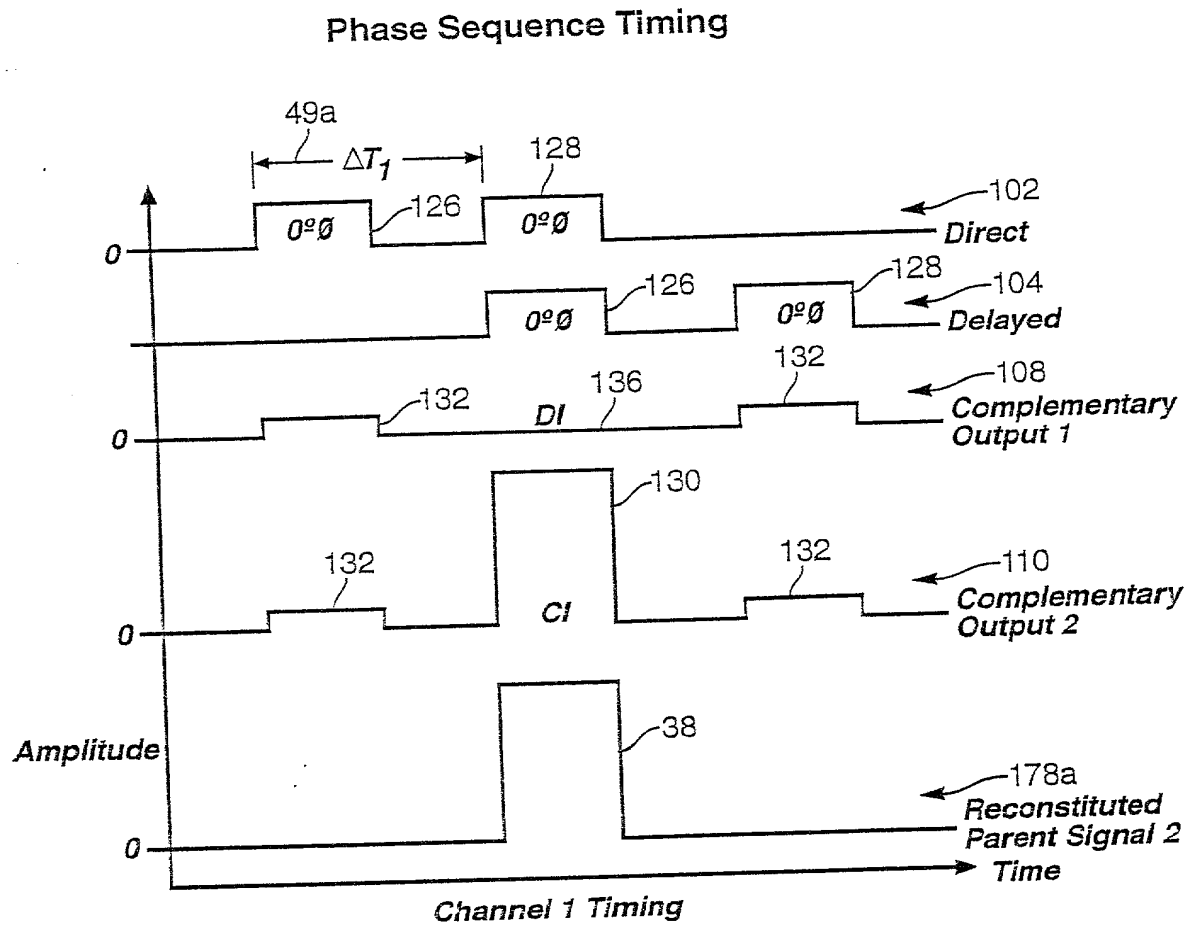


FIG. 32

Phase Sequence Timing

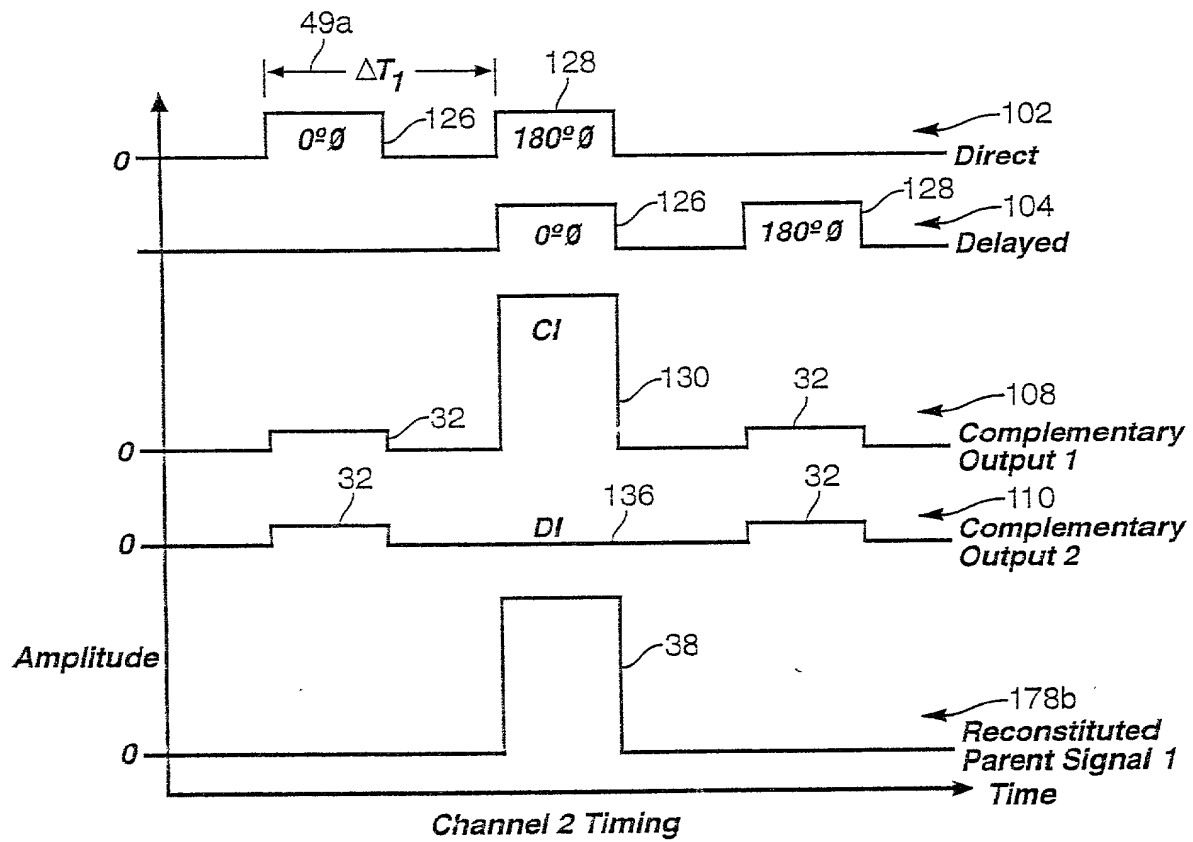


FIG. 33

Quadrature Encoding/Decoding Apparatus

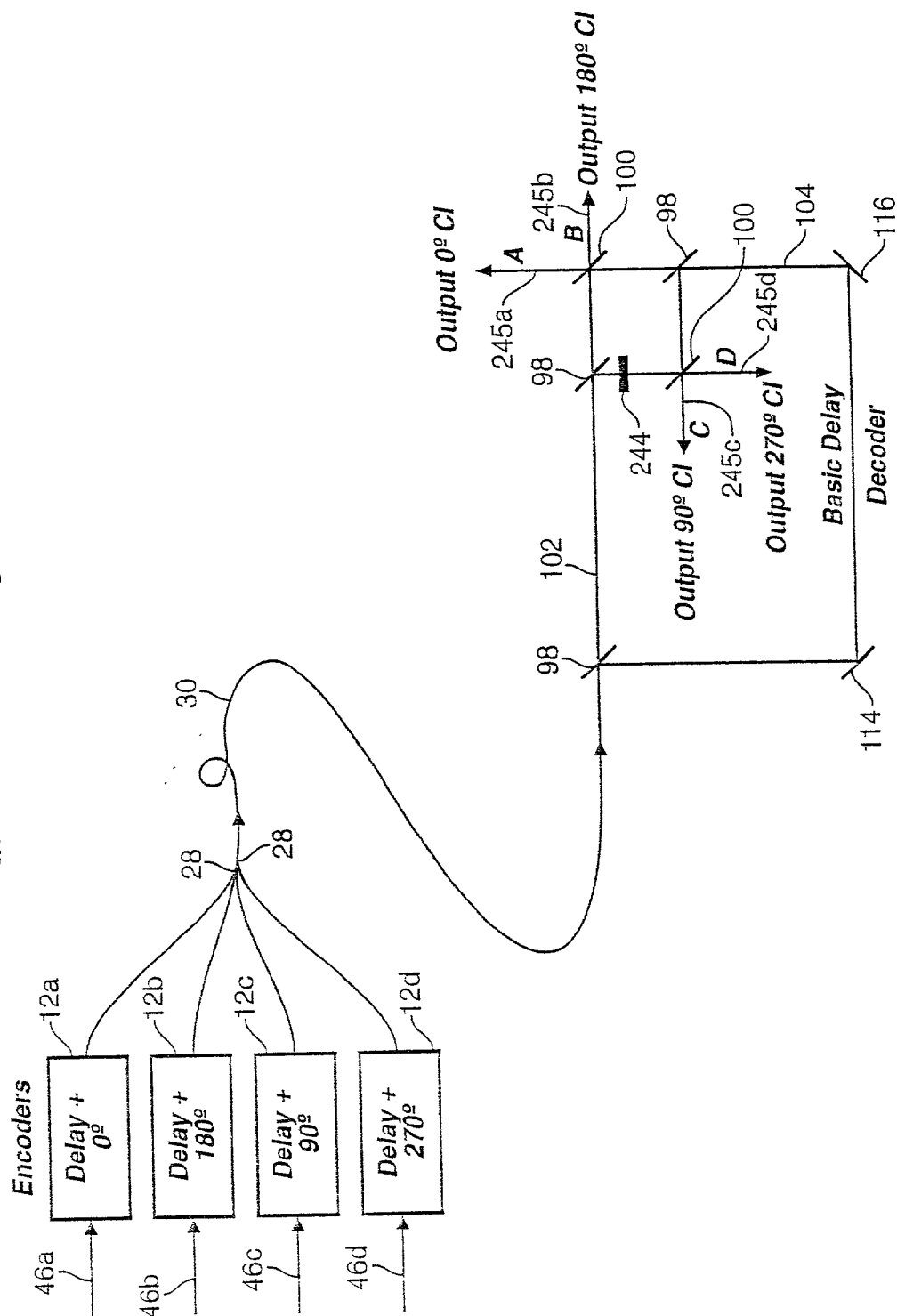


FIG. 34

	<i>Phase of Direct Signal</i>	<i>Phase of Delayed Signal</i>	<i>Quadrature Outputs</i>			
			<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
46a → <i>Channel 1</i>	0	0	<i>CI</i>	<i>DI</i>	<i>C = D</i>	
46b → <i>Channel 2</i>	0	180	<i>DI</i>	<i>CI</i>	<i>C = D</i>	
46c → <i>Channel 3</i>	0	90	<i>A = B</i>		<i>CI</i>	<i>DI</i>
46d → <i>Channel 4</i>	0	270	<i>A = B</i>		<i>DI</i>	<i>CI</i>

245a 245b 245c 245d

FIG. 35

Quadrature Wave Forms For One Channel

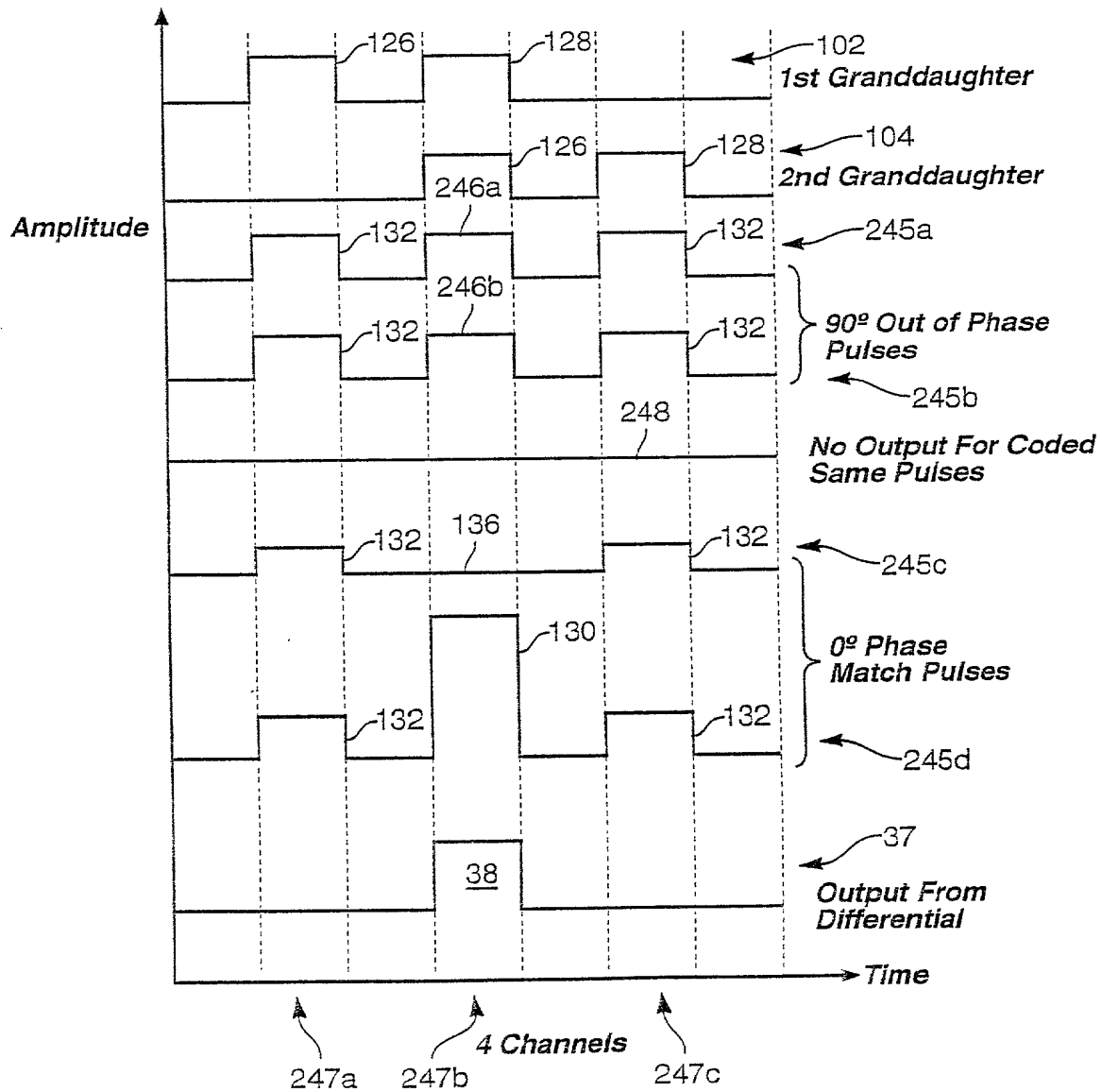


FIG. 36

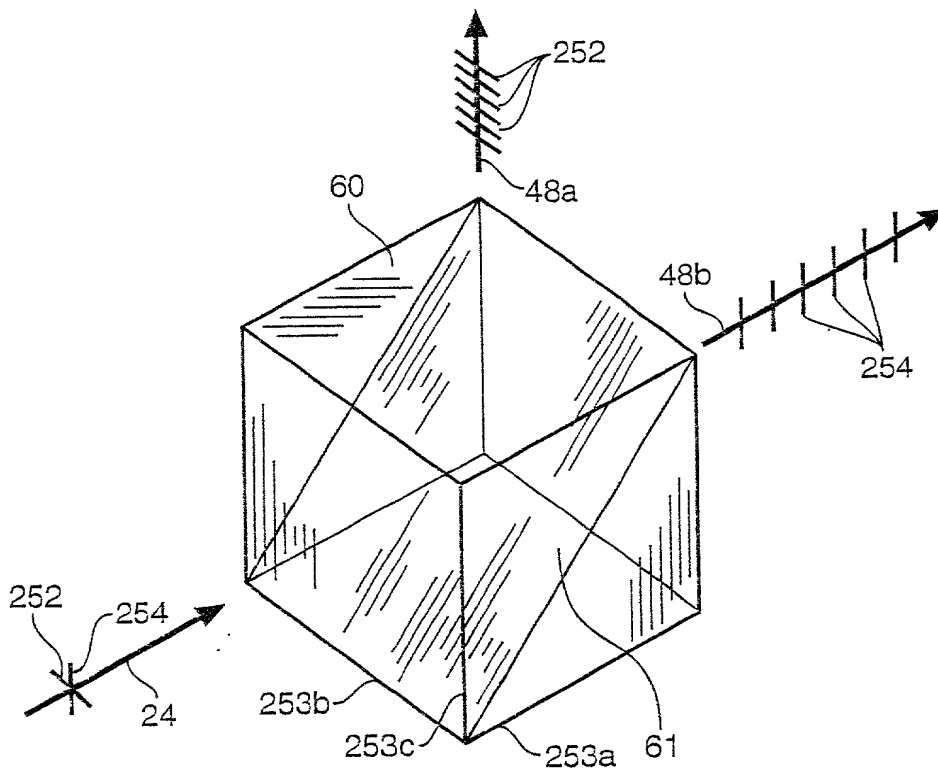


FIG. 37A

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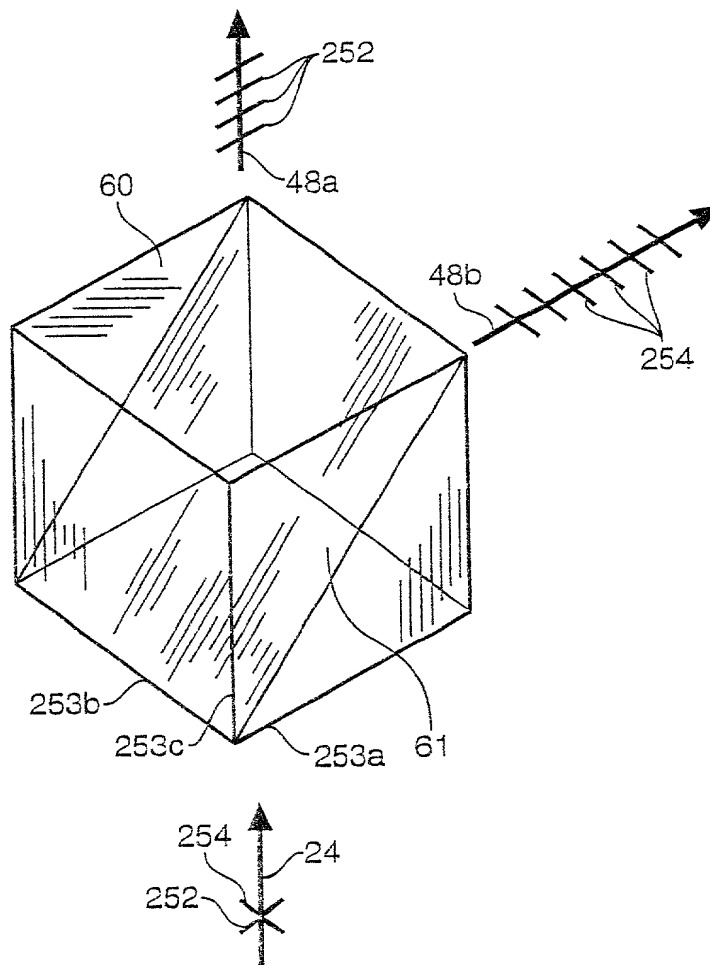
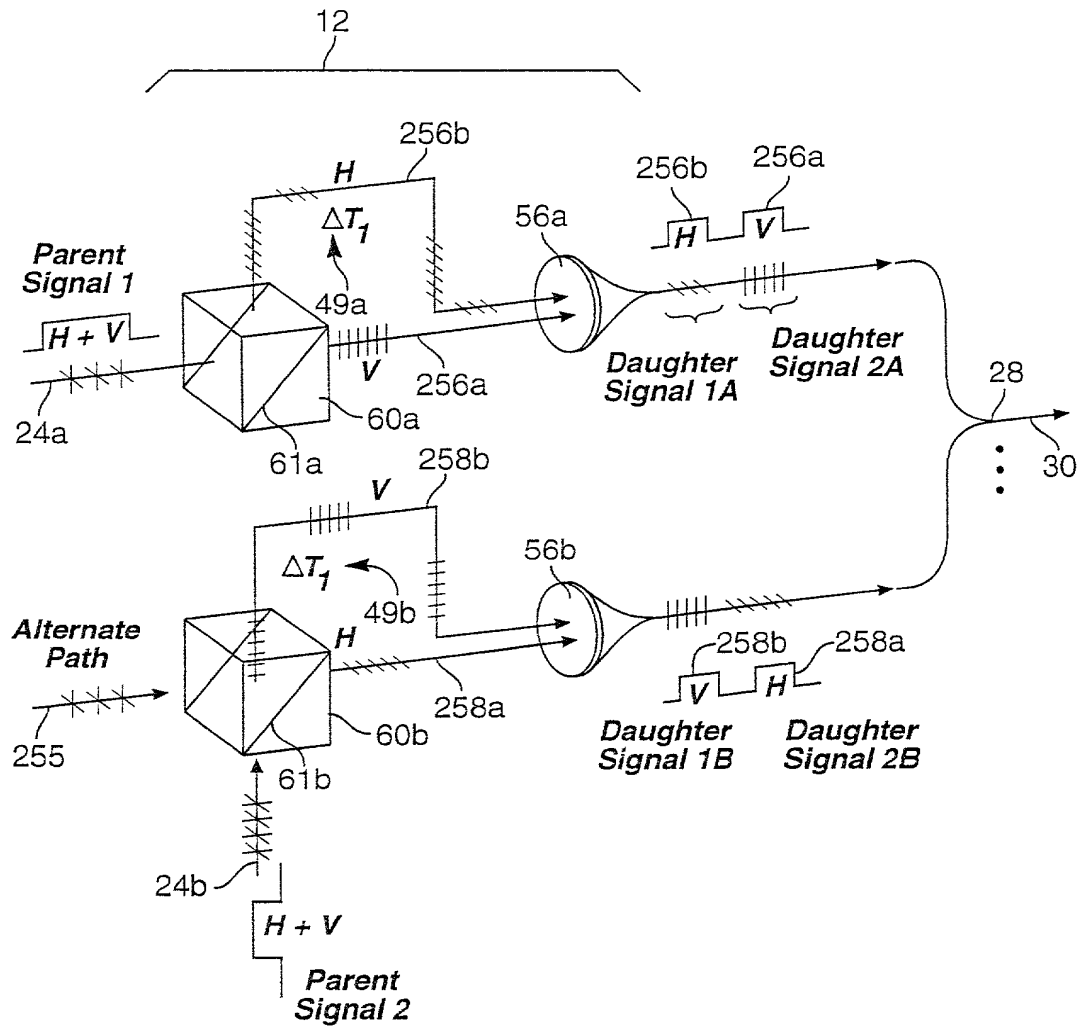
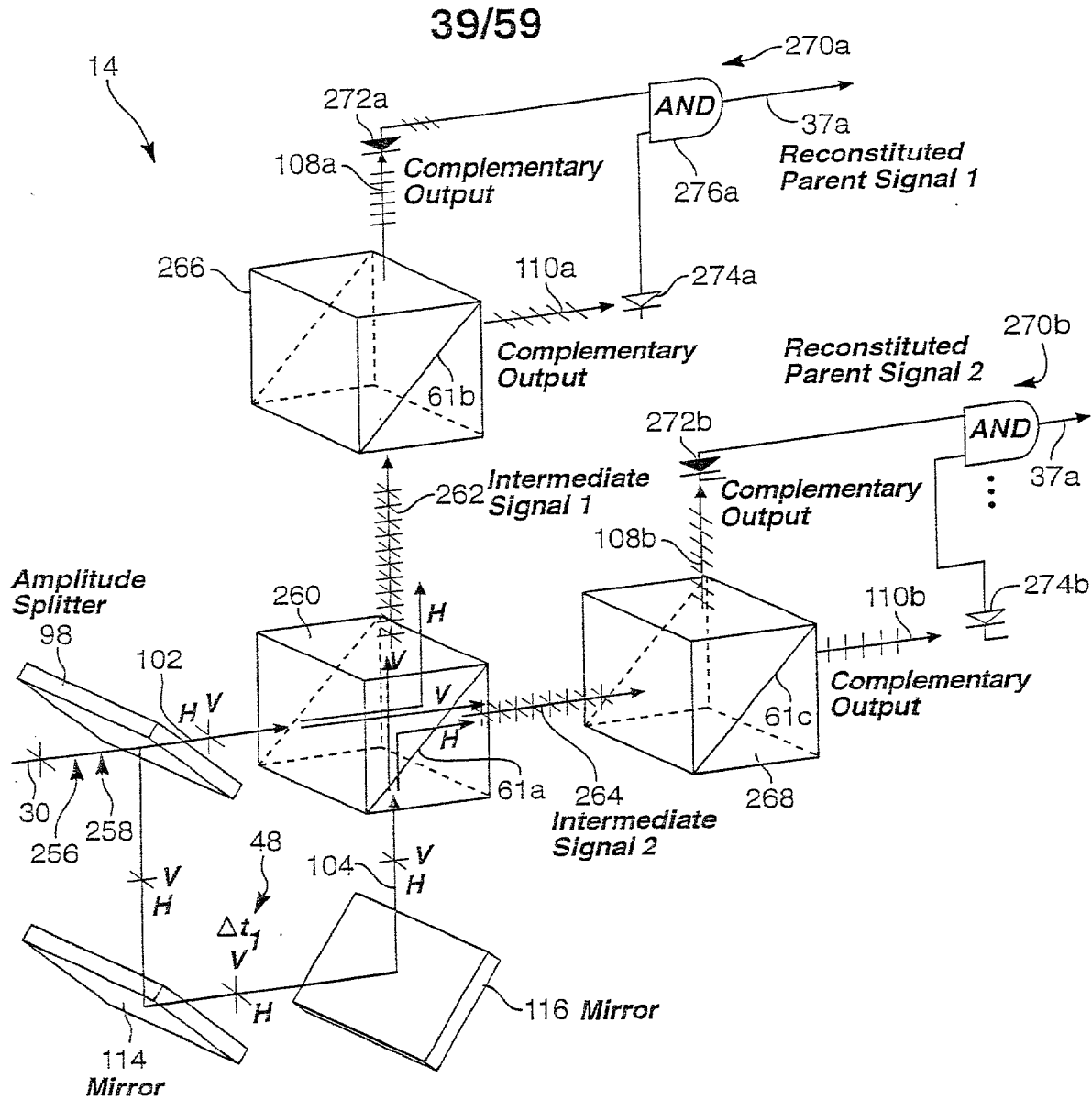


FIG. 37B



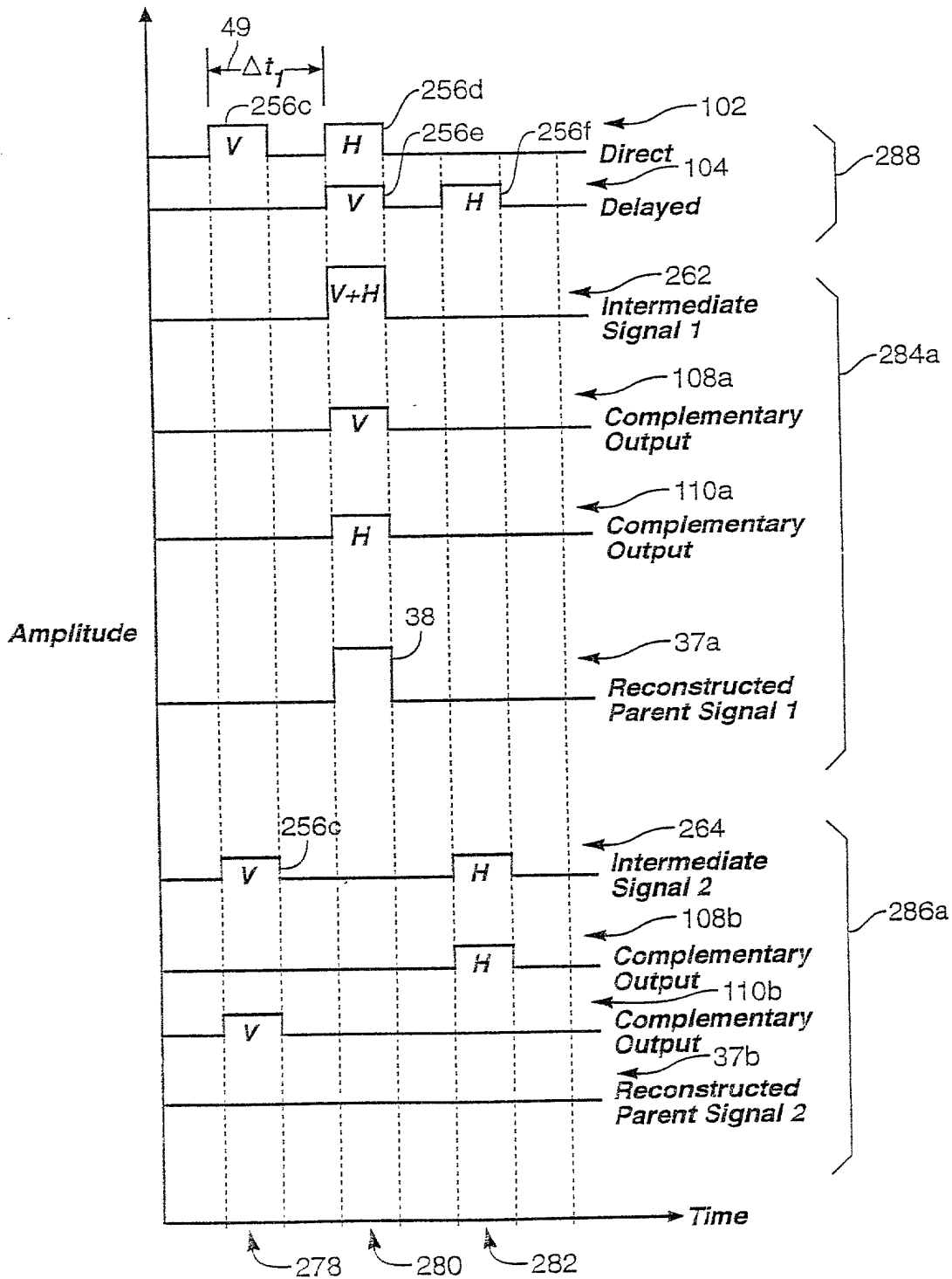
Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals

FIG. 38



**Double Decoder With Polarizations Sequenced
to Differentiate 2 Channels Having the Same Time
Delay Between Daughter Signals**

FIG. 39



Polarization Sequenced Channel 1 Timing

FIG. 40

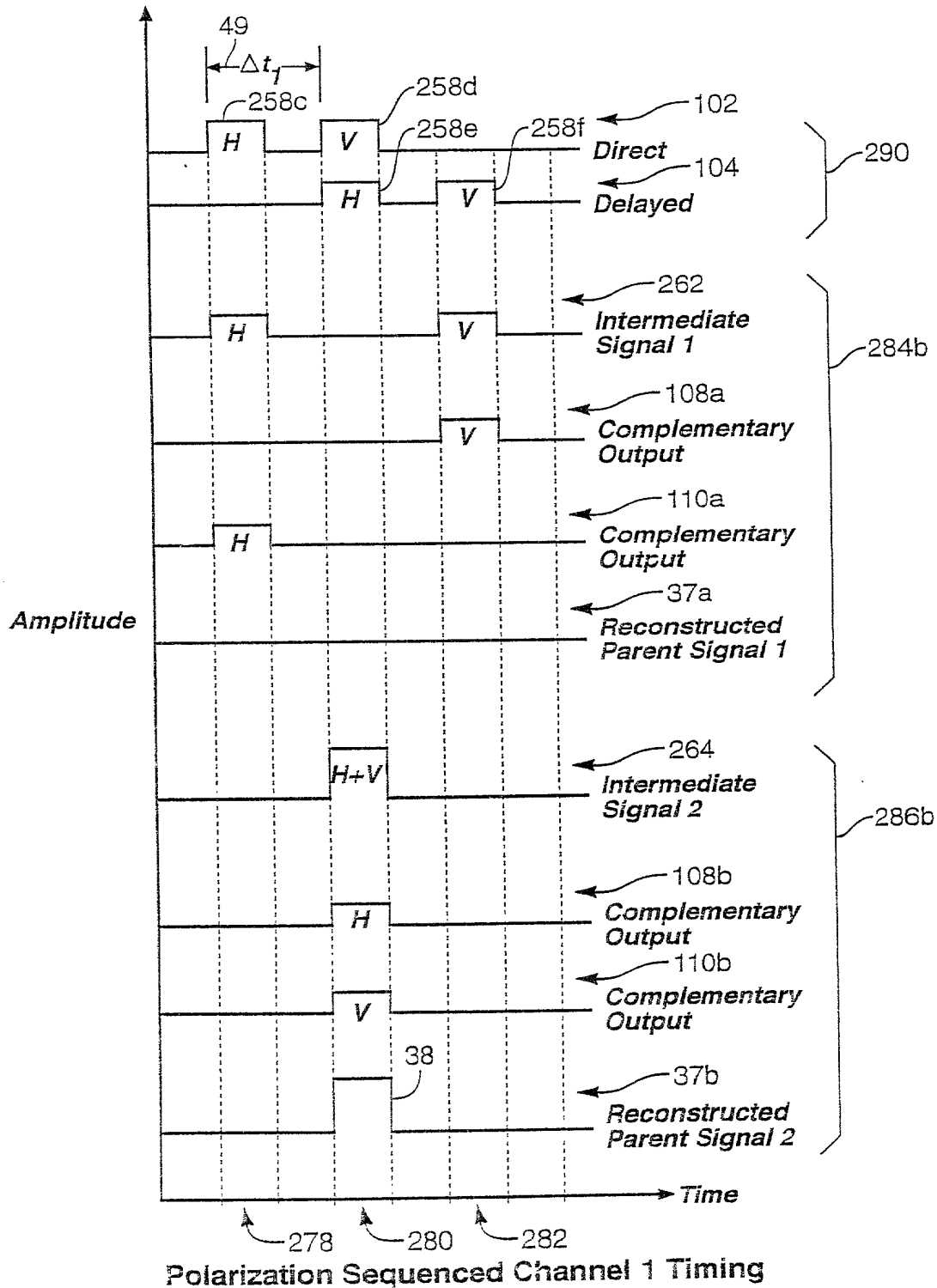


FIG. 41

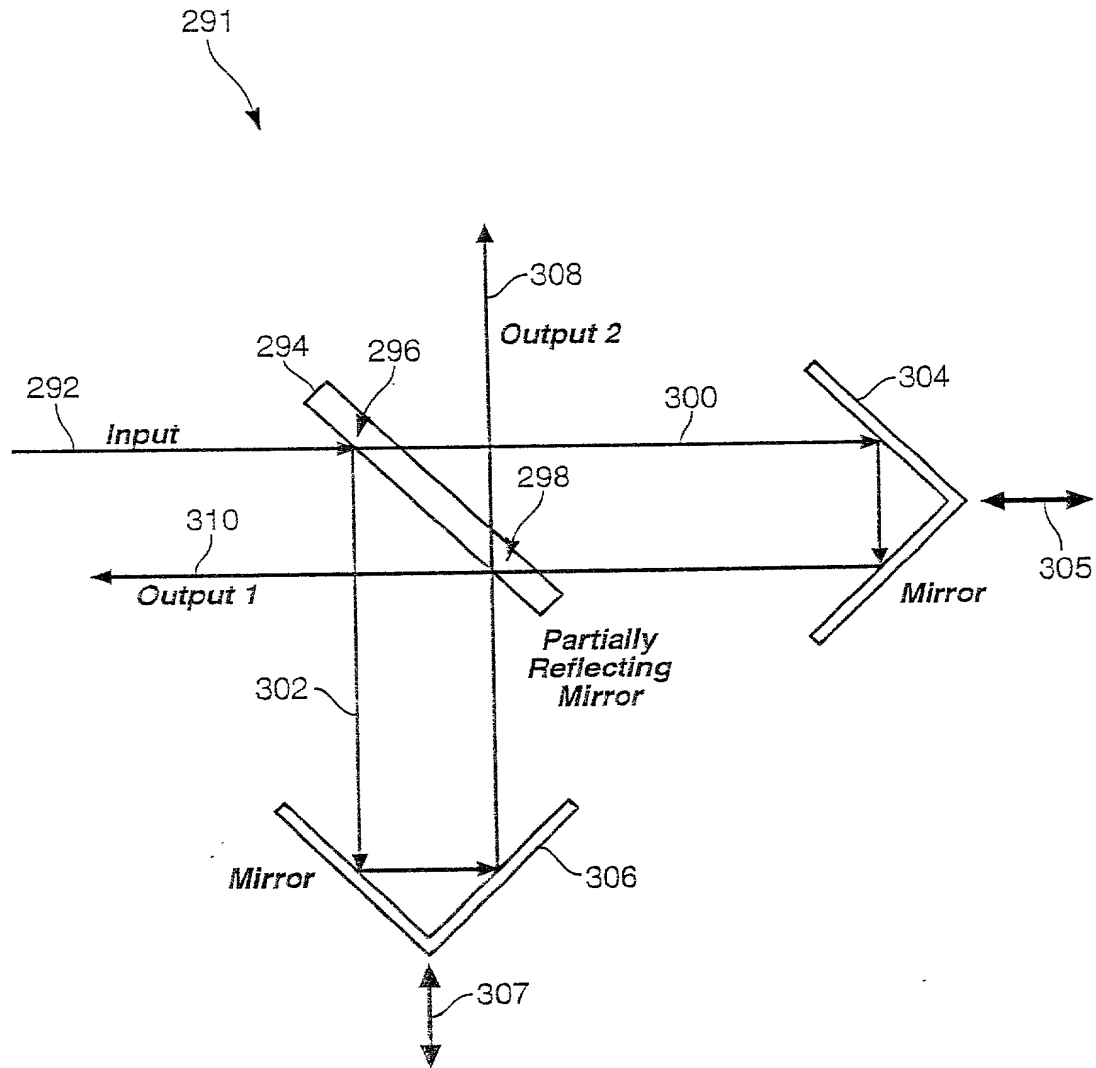


FIG. 42

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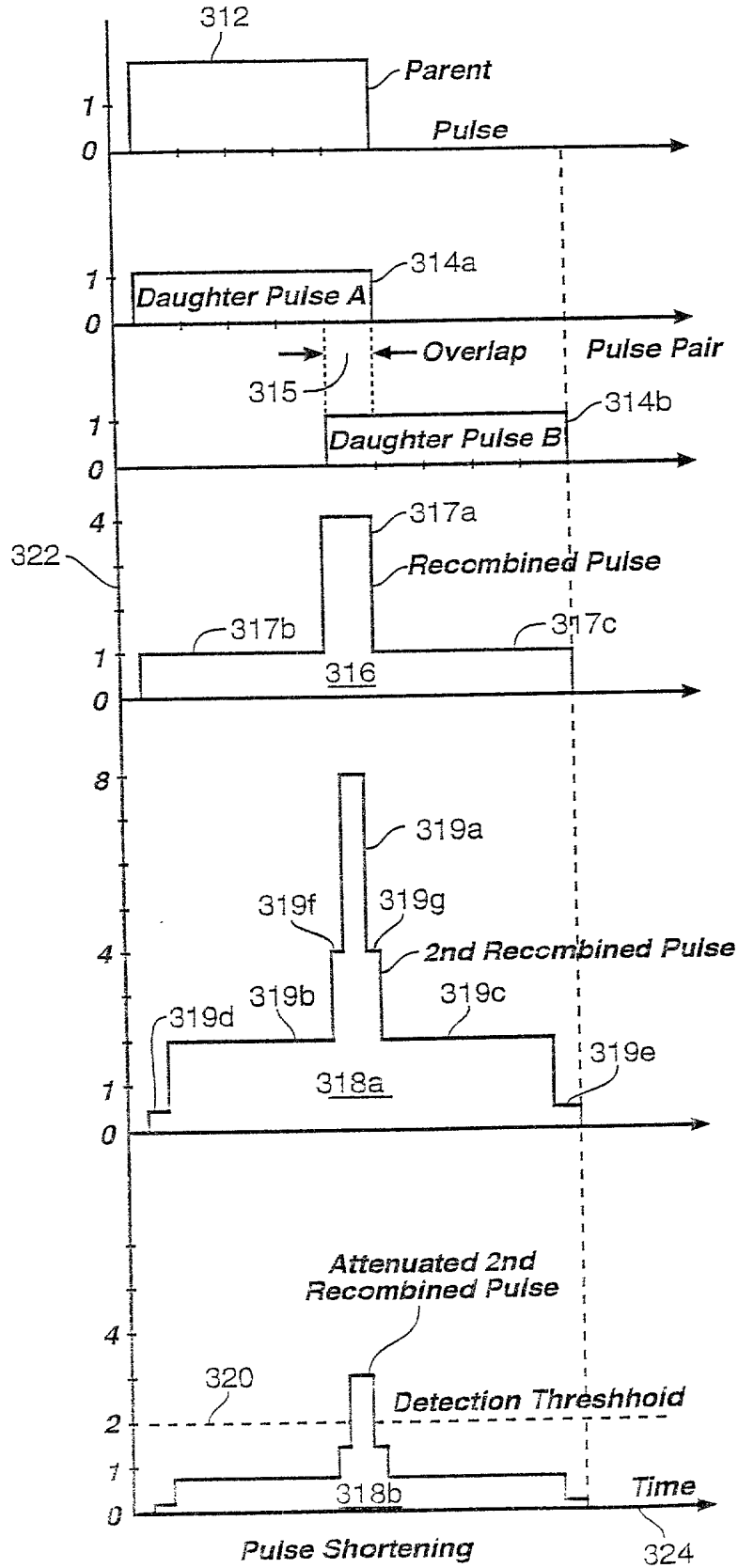


FIG. 43

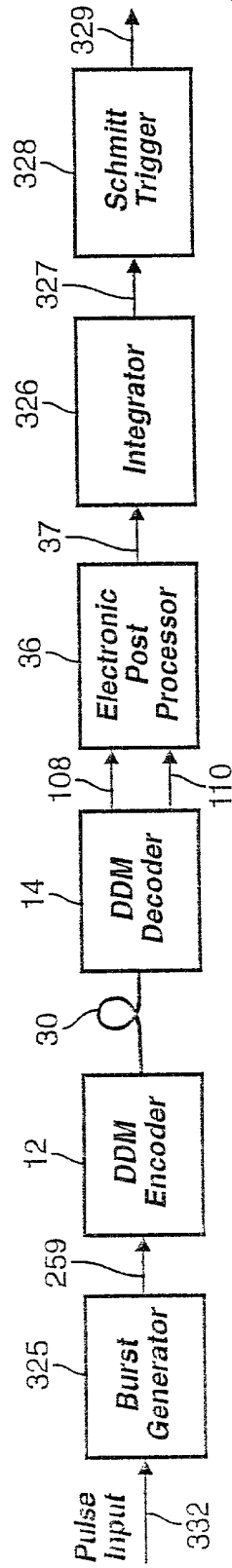


FIG. 44

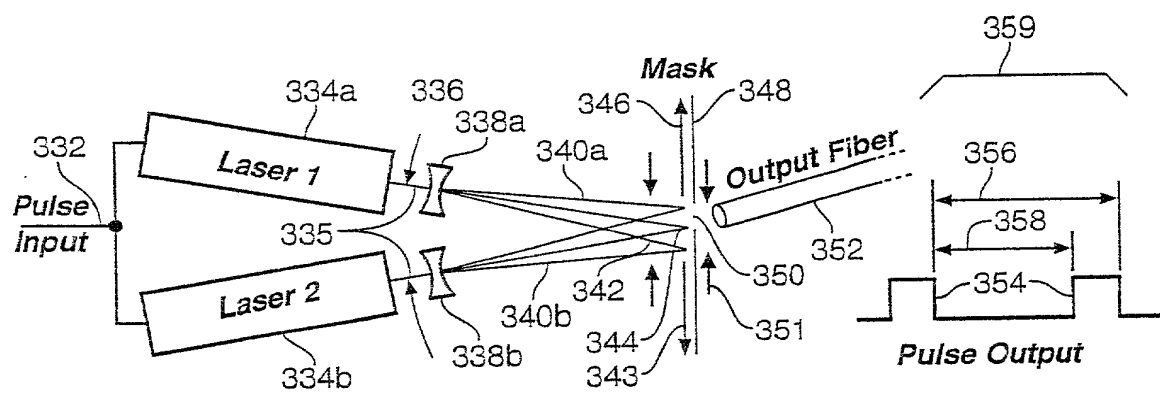


FIG. 45

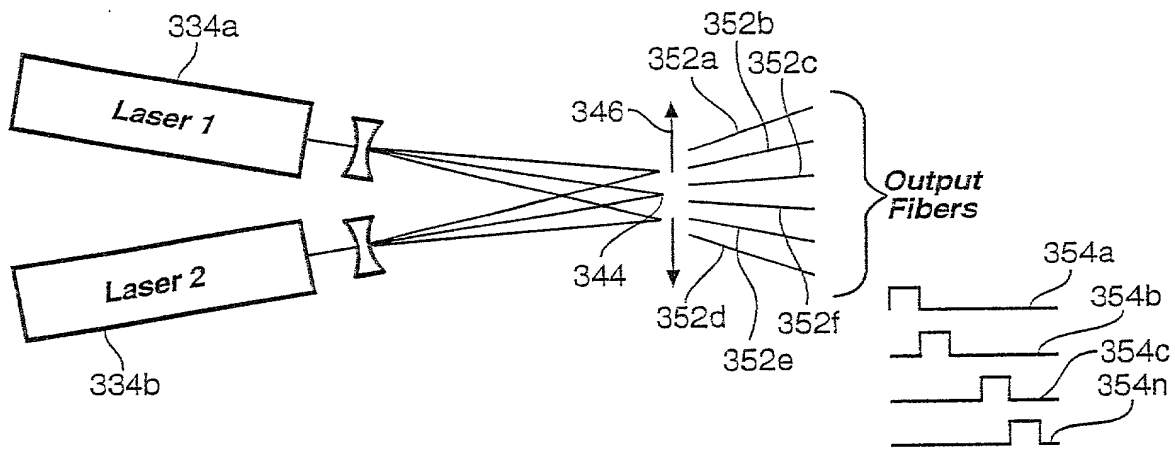


FIG. 46

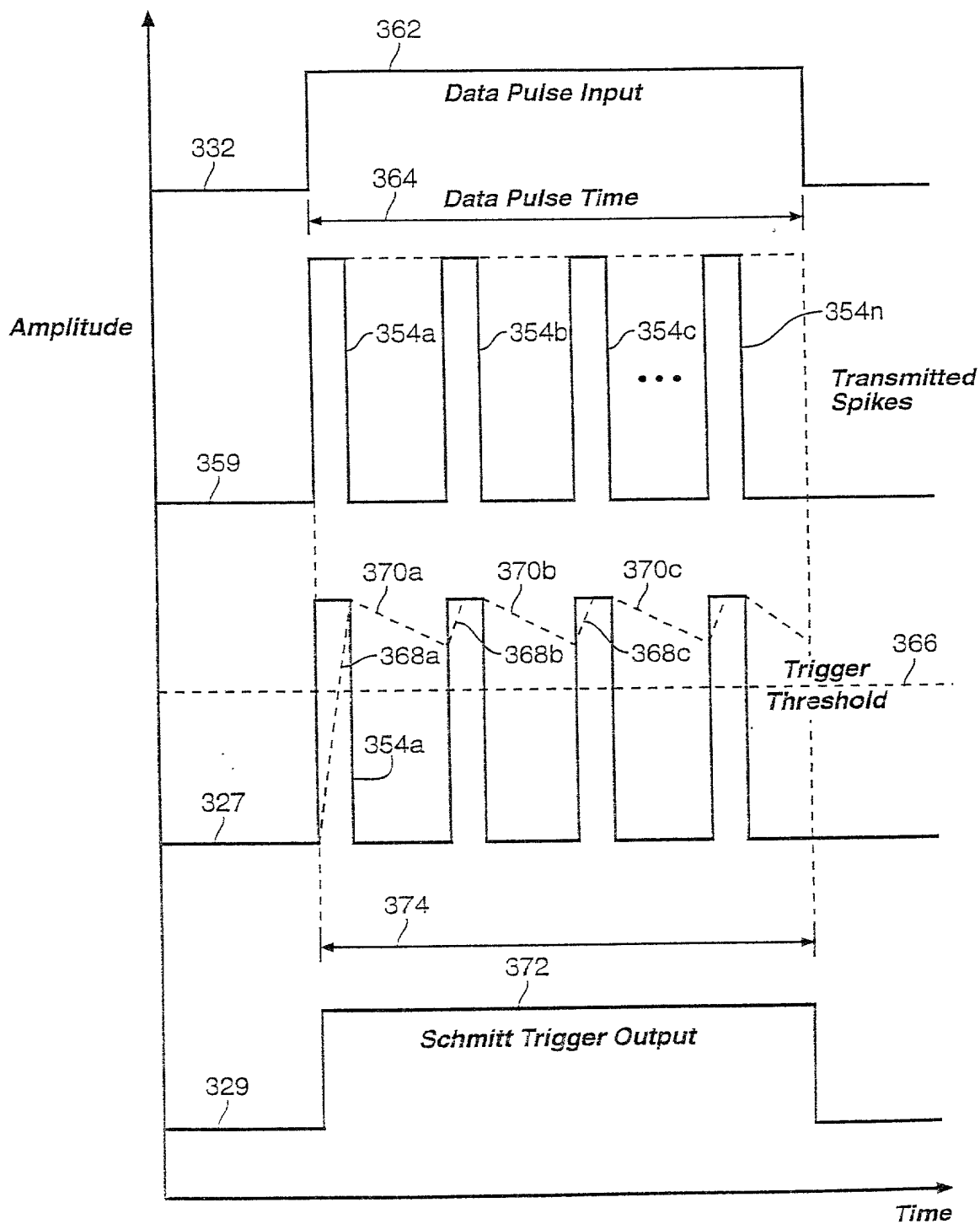


FIG. 47

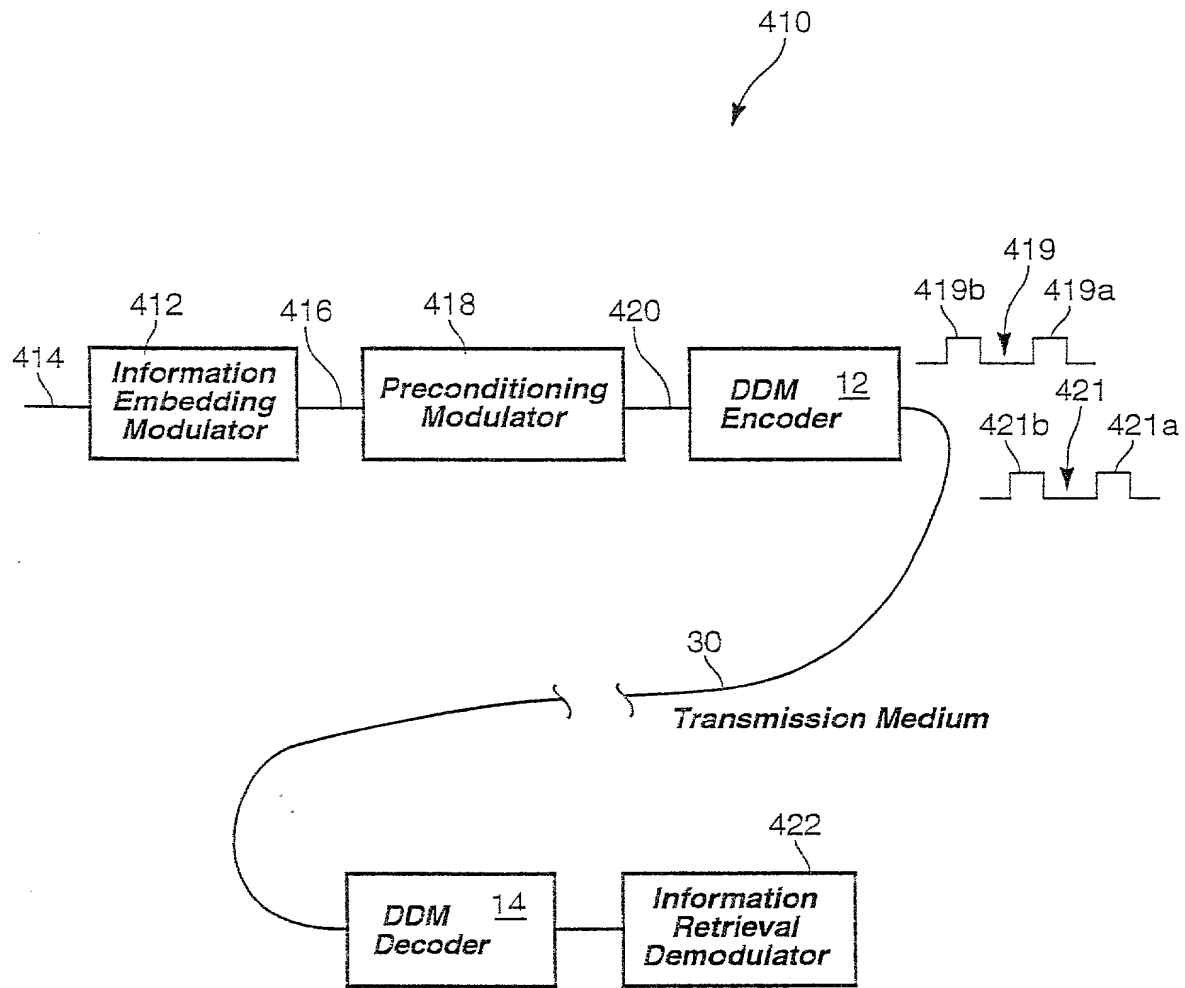


FIG. 48

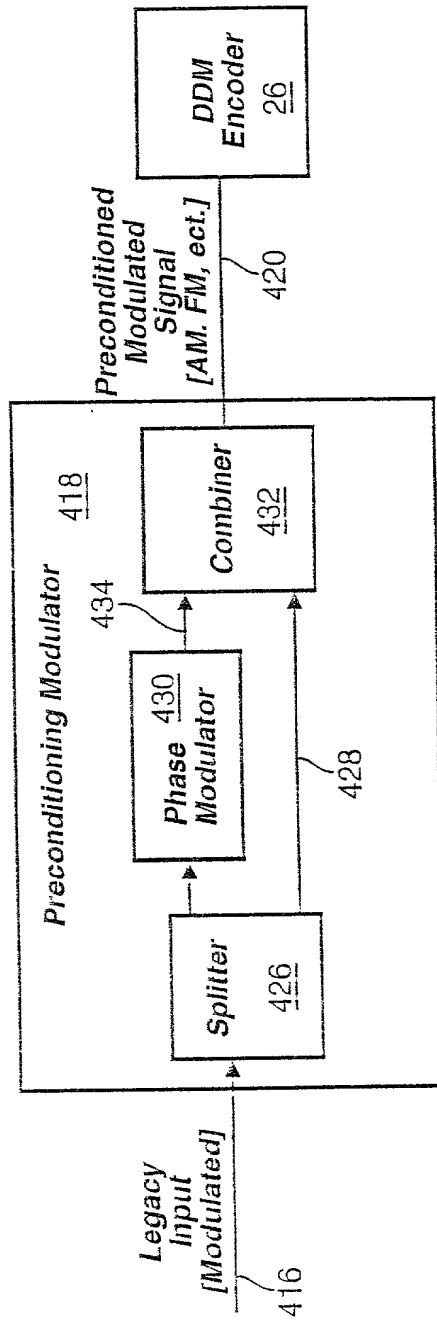


FIG. 49

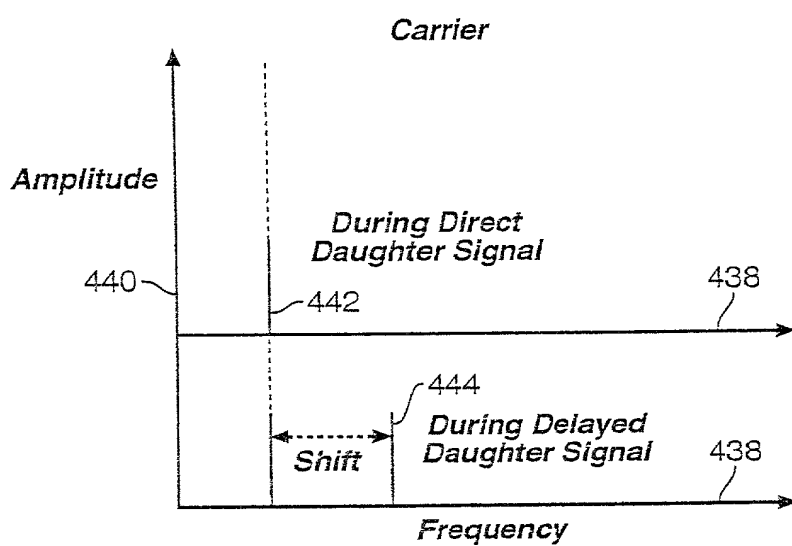


FIG. 50

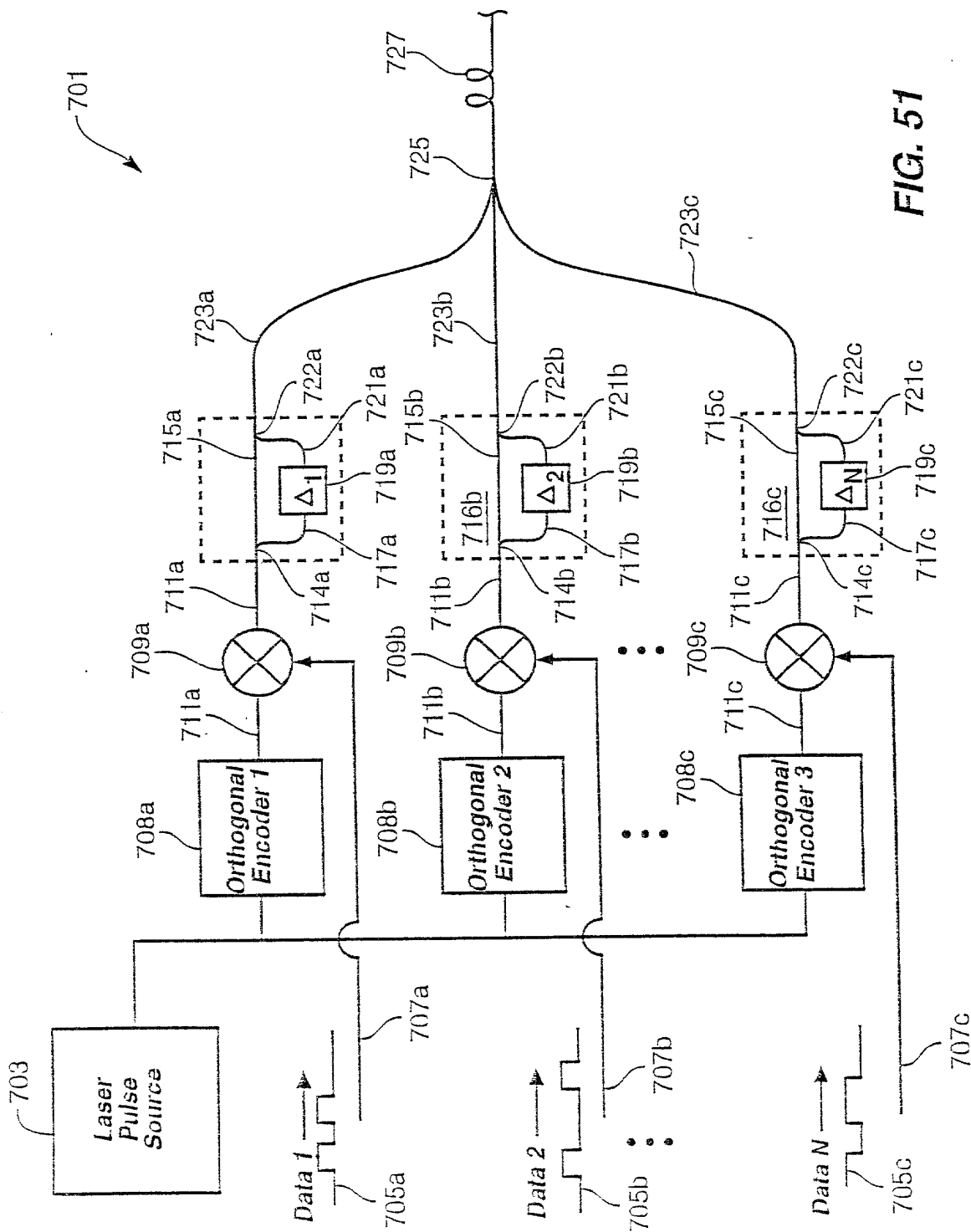


FIG. 51

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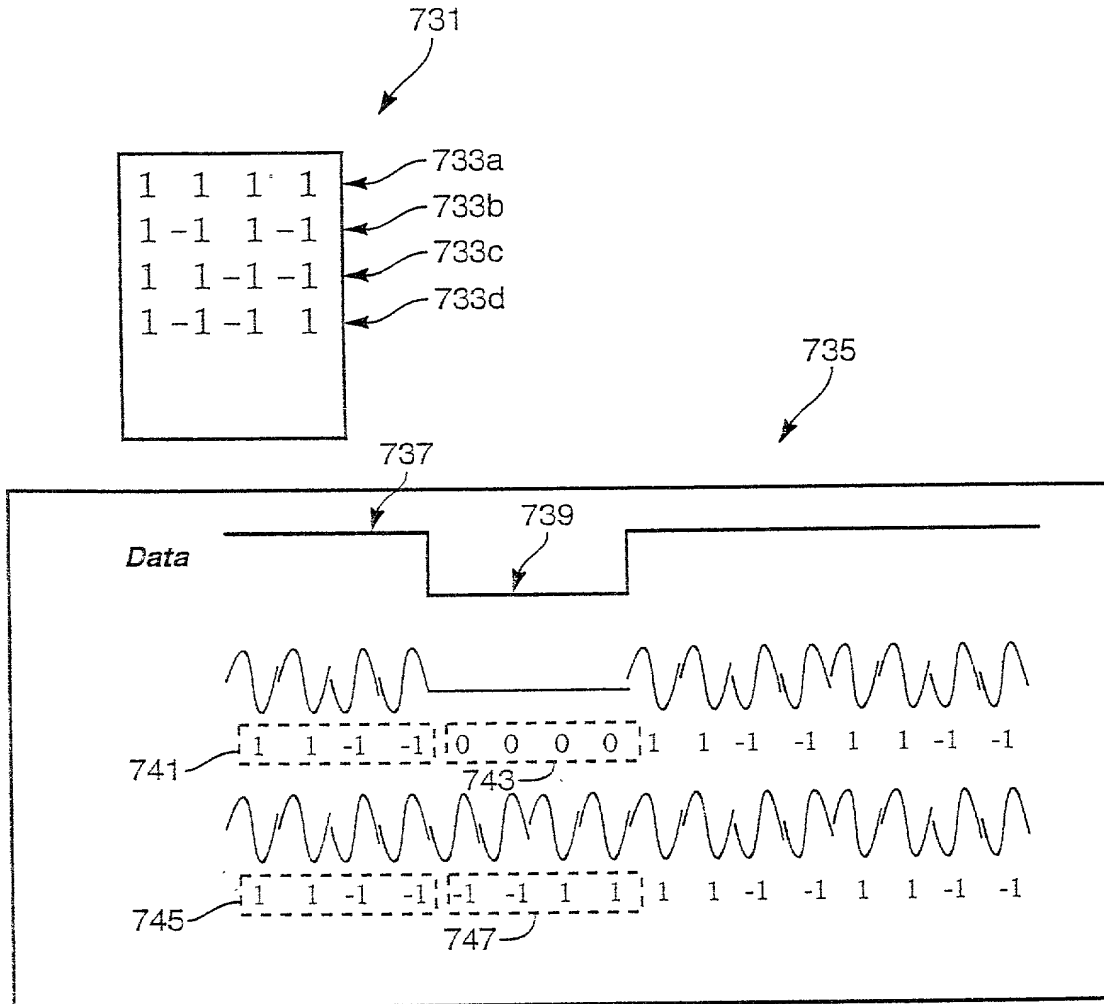


FIG. 52

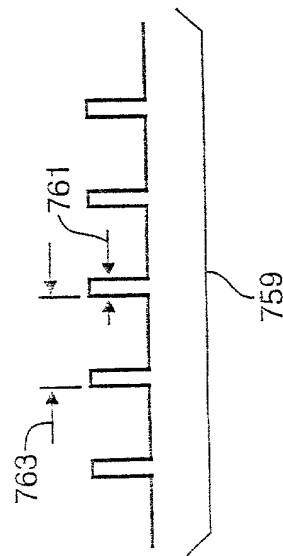
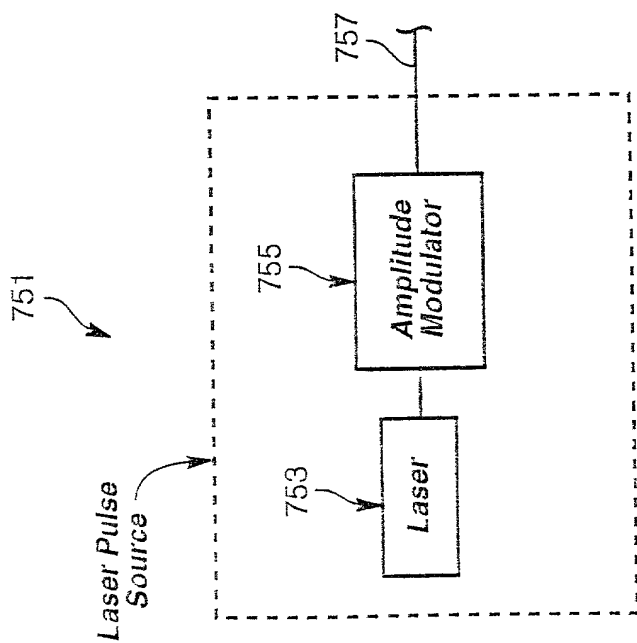


FIG. 53

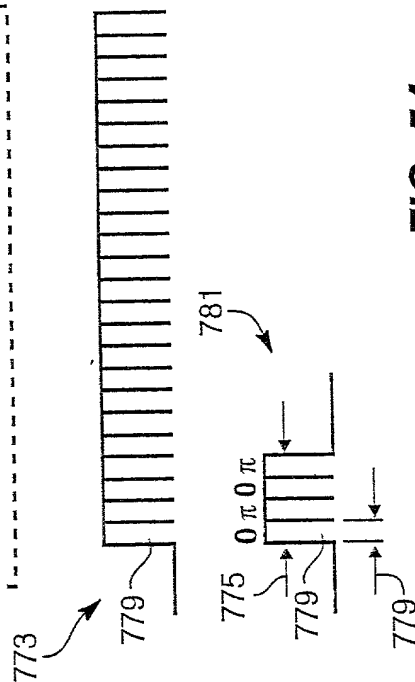
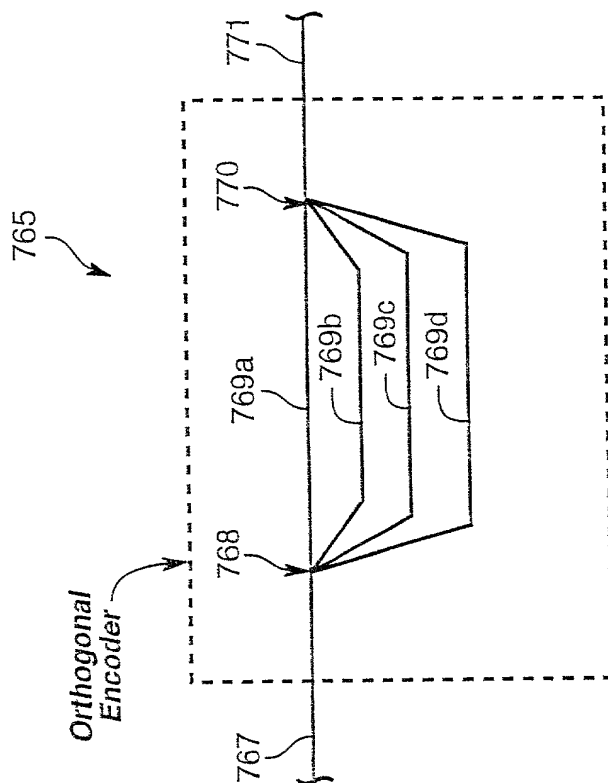
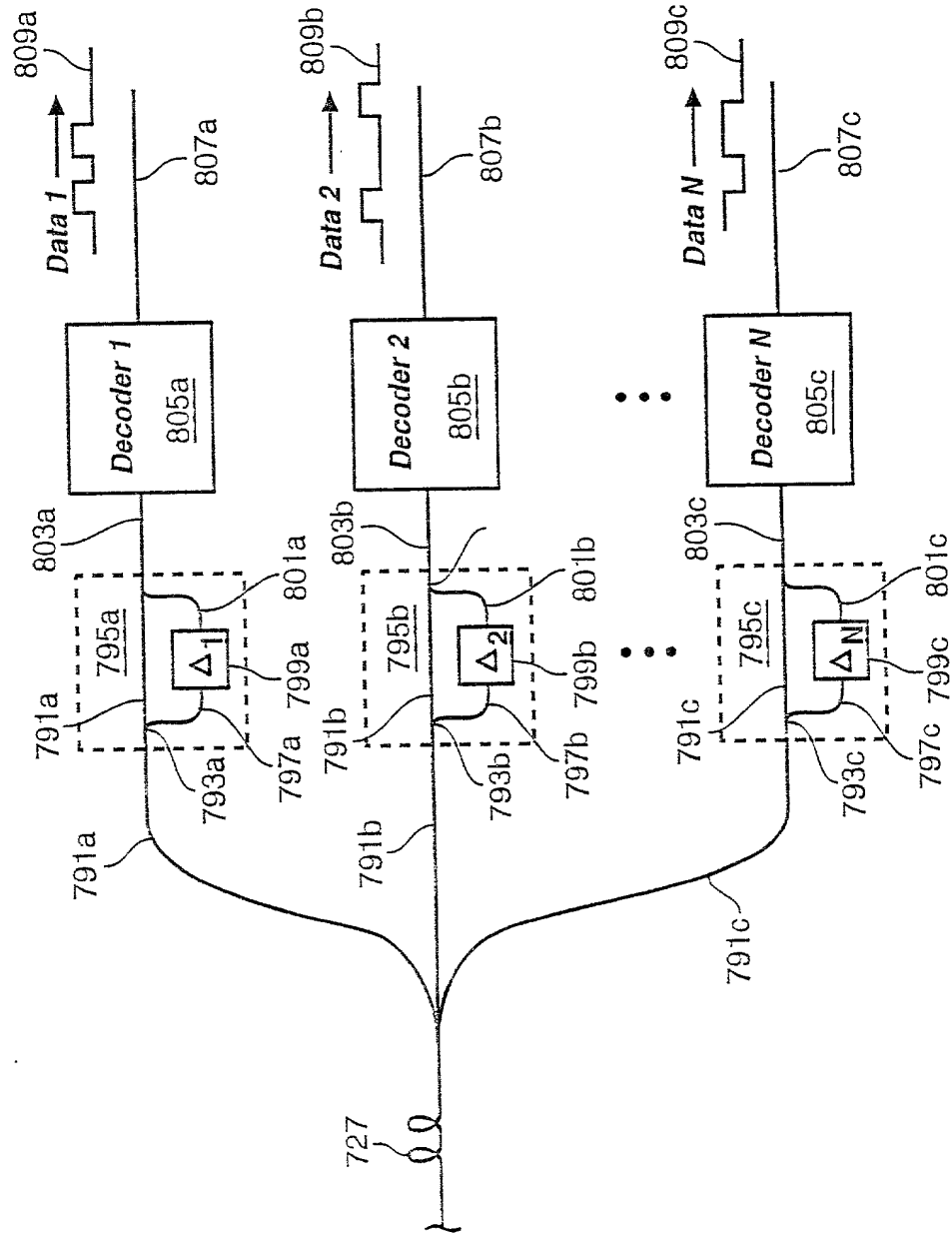


FIG. 54



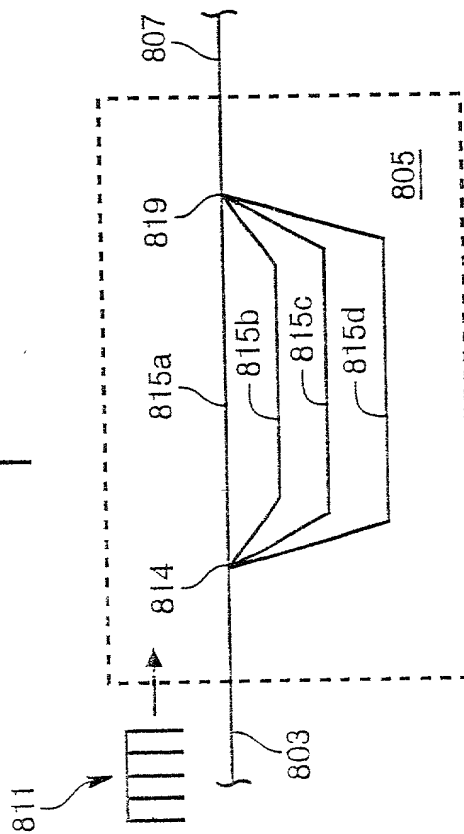
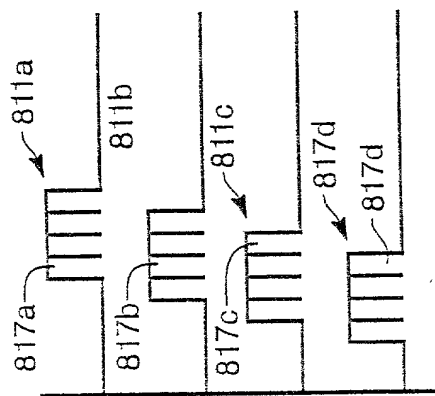


FIG. 56

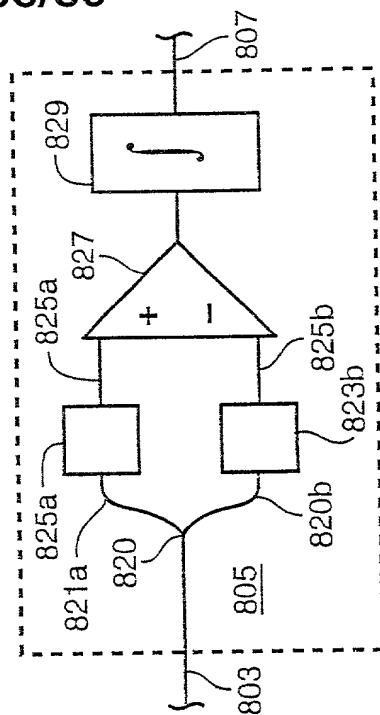


FIG. 57

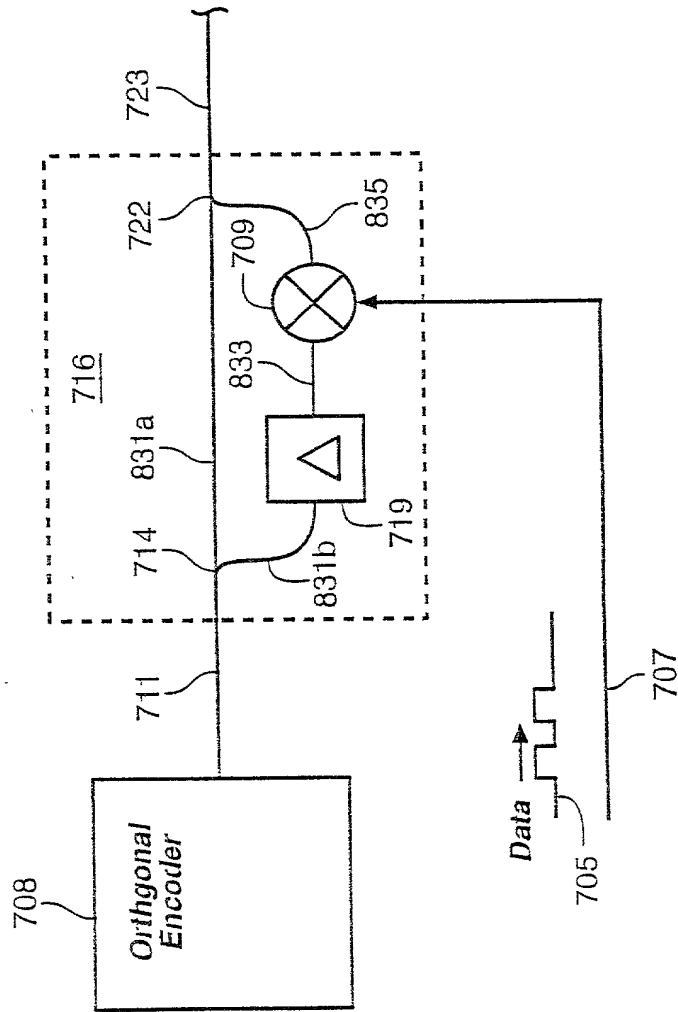


FIG. 58

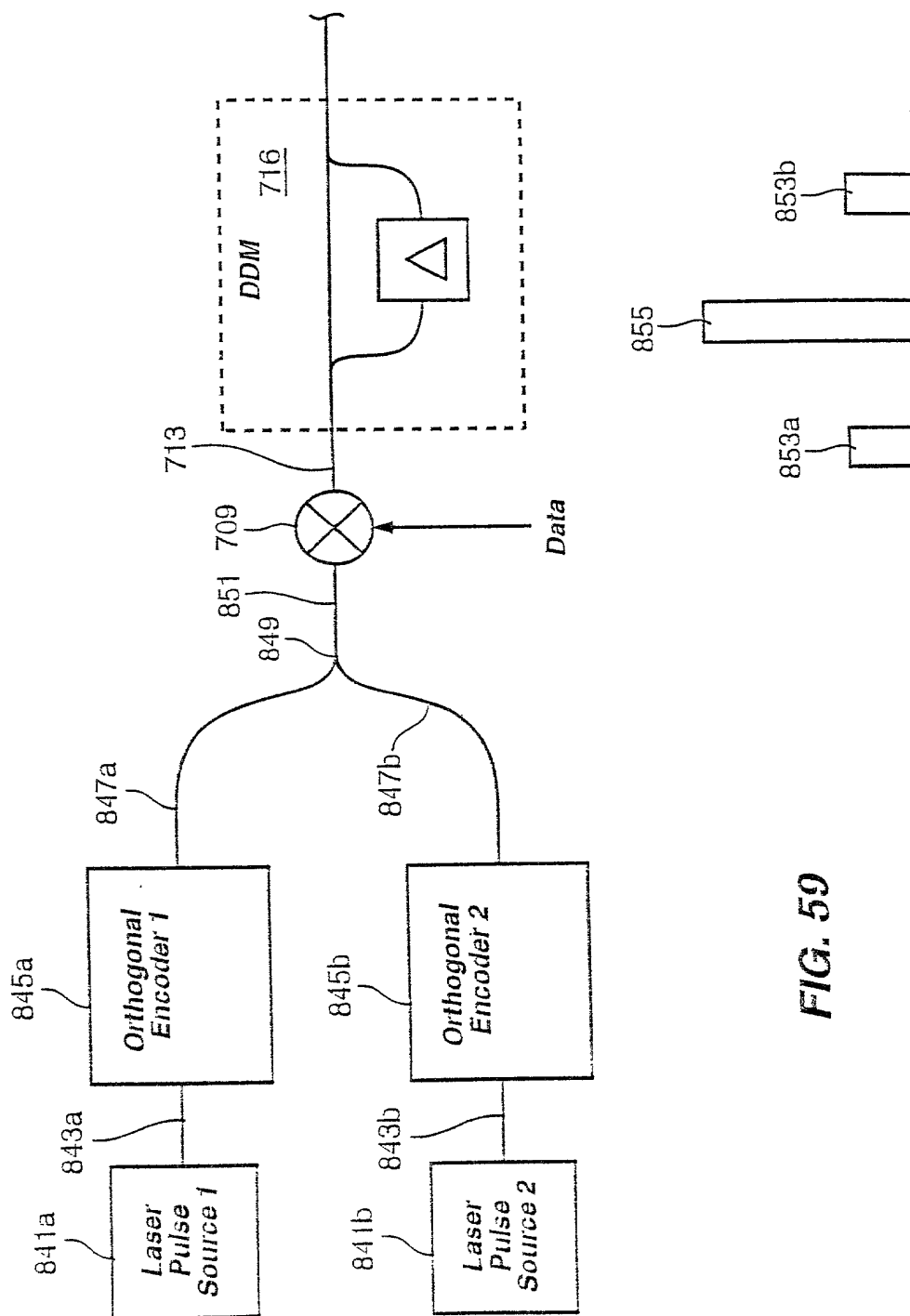


FIG. 59

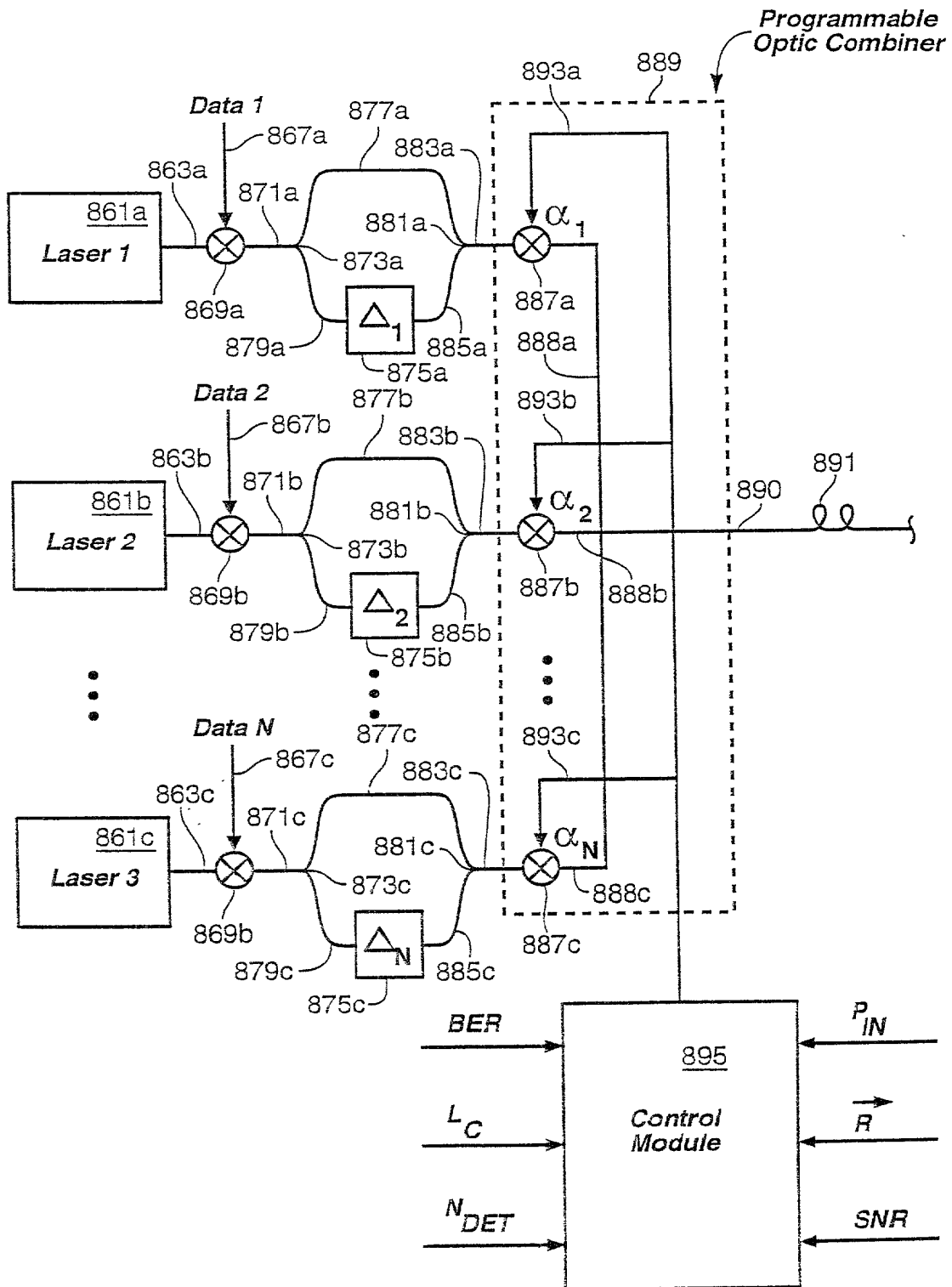


FIG. 60

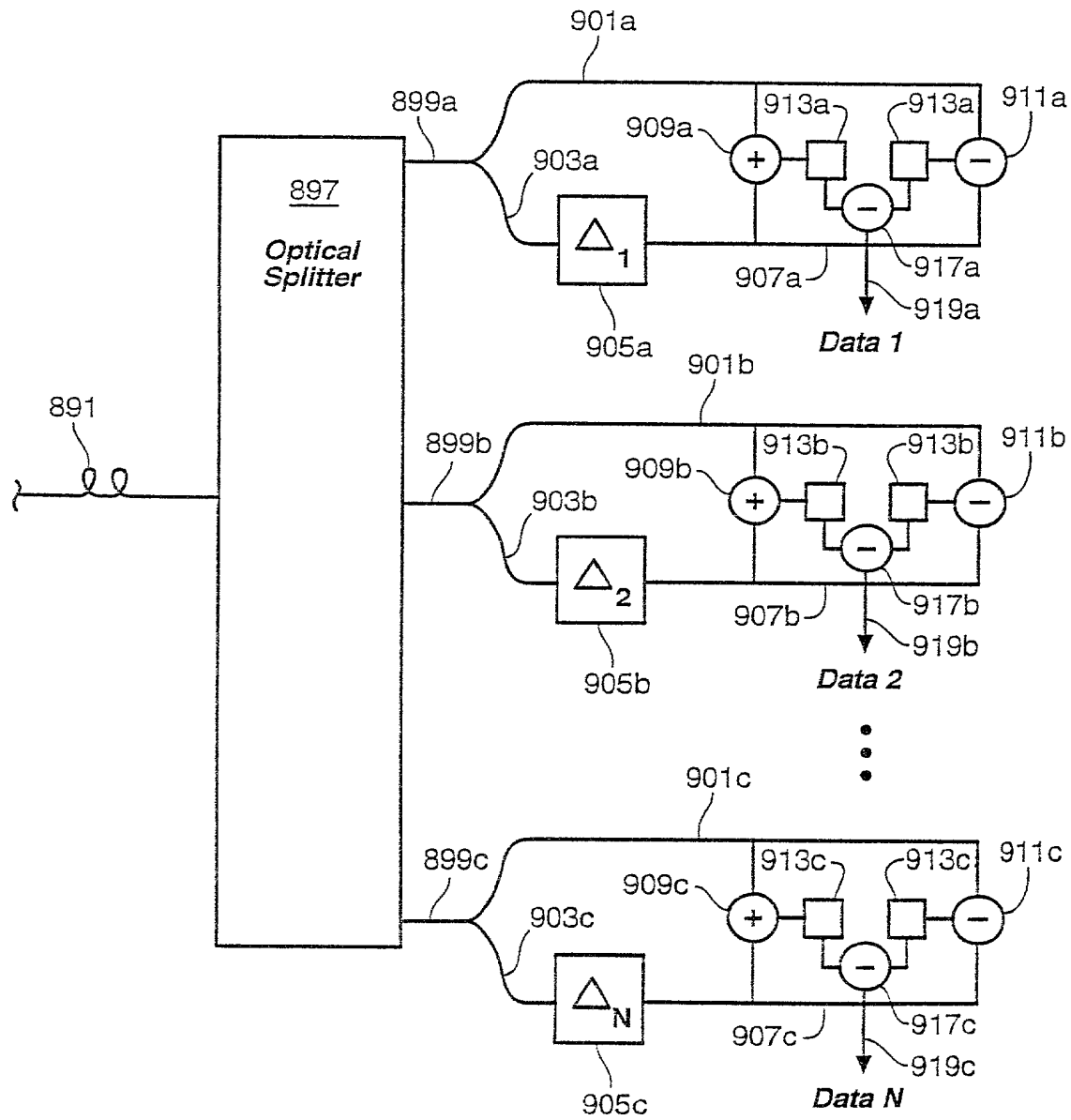


FIG. 61